Structure of the Technical Documentation

Register	Title	Remarks
1	User information	
2	Description	1. Key Interlock System 2. System Description 3. Technical Data 4. Operation 5. Setting the Operating Parameters 6. Functional Description 7. Functional Groups 8. Control Functions 9. Measurement and Monitoring 10. Monitoring the Input Circuit / Power Supply 11. Monitoring the Functioning of the RF Driver 12. Monitoring the Functioning of the Amplifier Module 13. Measuring and Monitoring the RF output Signal 14. Preparing for Operation 15. Maintenance
	Annex 1	Control Panel
	Annex 2	Fault Table
3	Circuit Diagrams	Circuit diagrams, numerically ordered see information on the next page
4	Component Layouts	Component layouts, numerically ordered see information on the next page
5	Parts List	Electrical parts list, numerically ordered

This manual presents the technical documentation for the medium wave transmitter type TRAM 100 and is registered under the documentation number **TFS 3029**. The bottom corner of the pages are labeled with a letter representing the revision index and the date. The revision index "a" signifies the initial release followed by the month and year.
Updates (revisions) to the initial release are identified by the revision index letter and the date.

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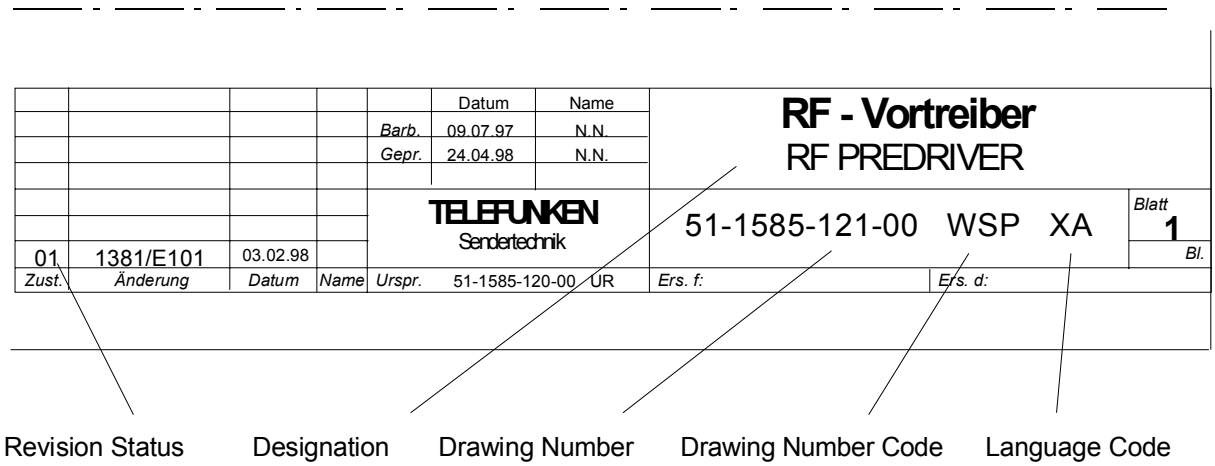
Information concerning Registers 3 and 4

Electrical drawings (Register 3) are identified in their title head by their designation, drawing number, drawing number code and language code. The first two or three letters after the drawing number identify the type of drawing. These letters may be followed by a two letter code indicating the language in which texts in the drawings are written.

Drawing Number Code		Language Code	
WSP	Circuit Diagram	*none*	German
BSP	Site Construction Drawing	**EL**	English
USP	Overview Drawing	**FZ**	French
STR	Interconnection Diagram	**SP**	Spanish
SHZ	Schematic Drawing	**XA**	German/English
LP	Cable Wiring Diagram	**XB**	German/English/French
NA	Retrofit Information		

Component layouts (Register 4) only have their designation in German, English and French followed by the code V8.

Example of a title head



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100 kW MEDIUM WAVE TRANSMITTER
TRAM 100

Technical Documentation

CONTENTS

CONTENTS

1. KEY INTERLOCK SYSTEM

The transmitter consists of five 19" cabinets provided with doors to enable easy access to the components inside. The doors behind which parts are under high voltage during operation are interlocked to ensure that the transmitter is first disconnected from power before the doors can be opened. The other doors can be opened without keys, since the voltage inside is either separately screened or not dangerous (≤ 24 V). Panels which can be removed with tools are not incorporated in the key interlock system.

1.1 Functioning of the Key Interlock

The transmitter is connected to the mains supply through a loadbreak switch (in the following termed the main switch). In order to engage the main switch, key A1 must be inserted in the lock next to it. When the main switch is engaged key A1 is mechanically blocked and cannot be removed.

C a u t i o n !

If during transmitter operation the door of an amplifier cabinet is opened with the "master key" the transmitter shuts down (main contactor trips) without issuing a fault indication. For this reason open door operation (test operation) is only possible when the short circuit contacts in the doors of the amplifier cabinet are deactivated beforehand i.e., with the transmitter in the OFF state. See also Fig. 7.4 - 1

Step	*Key*	*Procedure "Unlock" - Lock in reverse order*
1	A1	Disengage main switch - Remove key A1, insert in position A1 of the lock panel at the rear of the control cabinet and turn - Rotate lever of the grounding switch to position "grounded".
2	B	Key B1 can now be unlocked and removed followed by B2, B3, B4 and B5 only in this sequence. The "B" keys are mechanically blocked in the locks when the doors are open and can only be removed when the respective door is properly closed and locked.

1.2 Opening the Transmitter

The procedures below must be followed:

- Switch the transmitter off by pressing key S3 " O " in the control panel. This switches off the 270 V supply to the RF predriver, RF driver and the amplifier modules in the amplifier cabinets. After this occurs, a discharge circuit ensures that the filter capacitors of the amplifier modules are rapidly discharged. Observe this process at instrument P20 for both amplifier cabinets (see Annex 1). **The**

transmitter may only be opened after the capacitors have completely discharged! Use an appropriate voltage tester to check this condition when the amplifier cabinet door is opened.

- Isolate the mains supply to the transmitter by disengaging the main switch. Key A next to the main switch is now released. This key is used to release the grounding switch level of the lock panel at the rear of filter cabinet 2.

  Note: The lock panel is accessible after opening the rear door of filter cabinet 2 with the socket key. This door is not integrated in the key interlock system since the components inside are sepaerately screened.

  After the transmitter output is grounded, the keys B1, B2, B3, B4 and B5 can be removed. These keys can then be used to open the doors integrated in the key interlock system. After opening the respective doors, check all voltage carrying parts such as, for example, busbars with a voltage tester to ensure isolation.

Transmitter front panels may only be removed when the main switch is disengaged and the RF output is grounded - as described above. If the panel in front of the main switch is to be removed take special note of the danger shield. **Voltage may still be present at the main switch!**

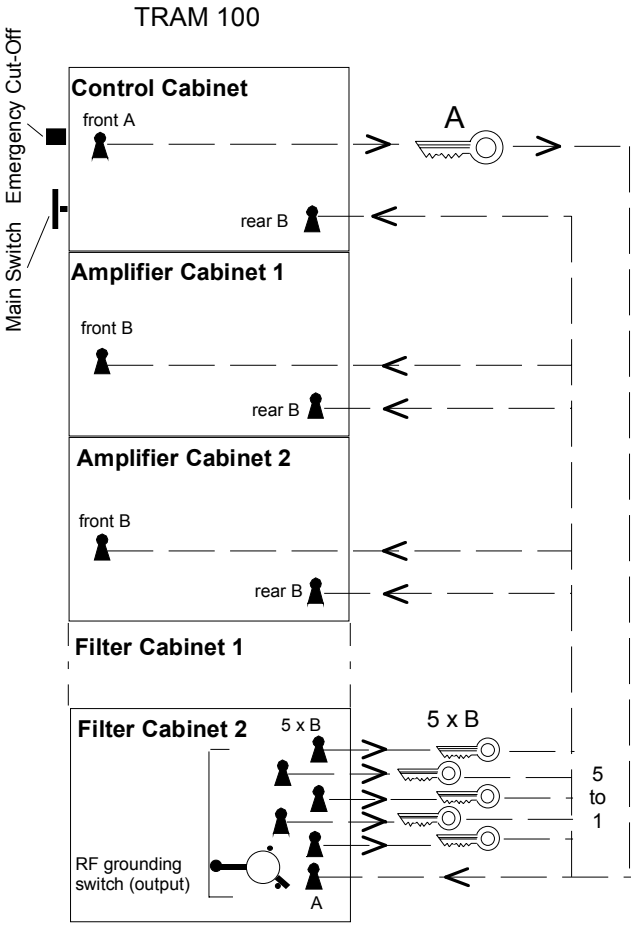

Fig. 1.1 -1: Key Plan

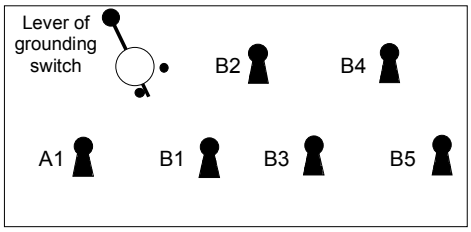

Fig. 1.1 -2: Lock Panel of Filter Cabinet 2

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1.3 Points to be noted when the Transmitter is opened:

- The main switch is protected by a cover panel, pay attention to the danger notice on the panel. The main switch behind this panel and may still be live.
- The grounding switch at the RF output is located in the filter cabinet 2 and protected against inadvertent touching. The grounding contact can be seen through the grid of the protective enclosure.
- When the door of the amplifier cabinet is opened, the current rails of the amplifier modules are connected to ground through the discharge resistors independent of the functioning of the discharge circuit.

1.4 Emergency Cut-Off Switch

The emergency cut-off switch isolates the transmitter from the mains power. The voltage supply for the emergency cut-off loop (24 V) and for the appliance socket (230 VAC) is independent of the transmitter feed.

2 SYSTEM DESCRIPTION

2.1 Amplifier Cabinets

Each amplifier cabinet accommodates a 50 kW power block comprising 48 amplifier modules and one drive module of the same type. Each amplifier module delivers over 1 kW of RF power into a special series transformer circuit (combiner) which sums the powers of all modules to the total output power of the transmitter. Each module is designed as a single plug-in pc board incorporating a switched RF amplifier bridge and an associated PDM modulation amplifier. Thus each module is a completely self-sufficient amplitude modulated RF amplifier. This has the advantage that in case of a module failure, transmitter operation is maintained at only slightly reduced power without affecting signal quality. If a faulty module is removed, it must be replaced by a spare or substituted by a dummy module. The drive module is driven by an RF amplifier which in turn is driven by the RF predriver. The RF predriver receives its input signal either from an external RF generator or the internal synthesizer board.

2.2 Filter Cabinets

Downstream of the 100 kW power block is a common output filter circuit accommodated in two 19" cabinets. The filter circuit is designed so that it can be tuned, within a permissible tolerance, to a mismatched load impedance (antenna) without a reduction in output power. The transmitter is equipped for and tuned to a pre-determined operating frequency.

2.3 Control Cabinet

The control cabinet contains the mains-feed connecting point with the main switch and the electrical distribution network for the transmitter components as well as auxiliary power supply units. In addition, it contains the control board, a control panel for local operation and metering to measure current, voltage, RF power, mismatch, RF phase and modulation. Other components installed in the control cabinet include the synthesizer board, the AF stage in which the PDM control signals are processed and the output monitoring circuit.

2.4 AF- and PDM Processing

The PDM control signals are processed in the AF stage and then distributed to the amplifier modules.

2.5 RF Drive

The transmitter is equipped with a common RF drive unit (synthesizer board) for all power modules. As an alternative, the RF drive signal can also be provided by an external frequency generator. Switchover to an external source is by means of a jumper on the synthesizer board.

2.6 Power Supply

All amplifier modules, the RF predriver and drivers are supplied by two 100 kVA transformer and four three-phase bridge rectifier installed in the lower part of the amplifier cabinets.
A 24 V switched power supply feeds the fan tray units and the relays. Three auxiliary power supplies deliver various voltages to most of the transmitter components.

2.7 Cooling System

The transmitter is exclusively air cooled. A fan tray unit is arranged below the power modules in each amplifier cabinet to force cooling air over their heat sinks.

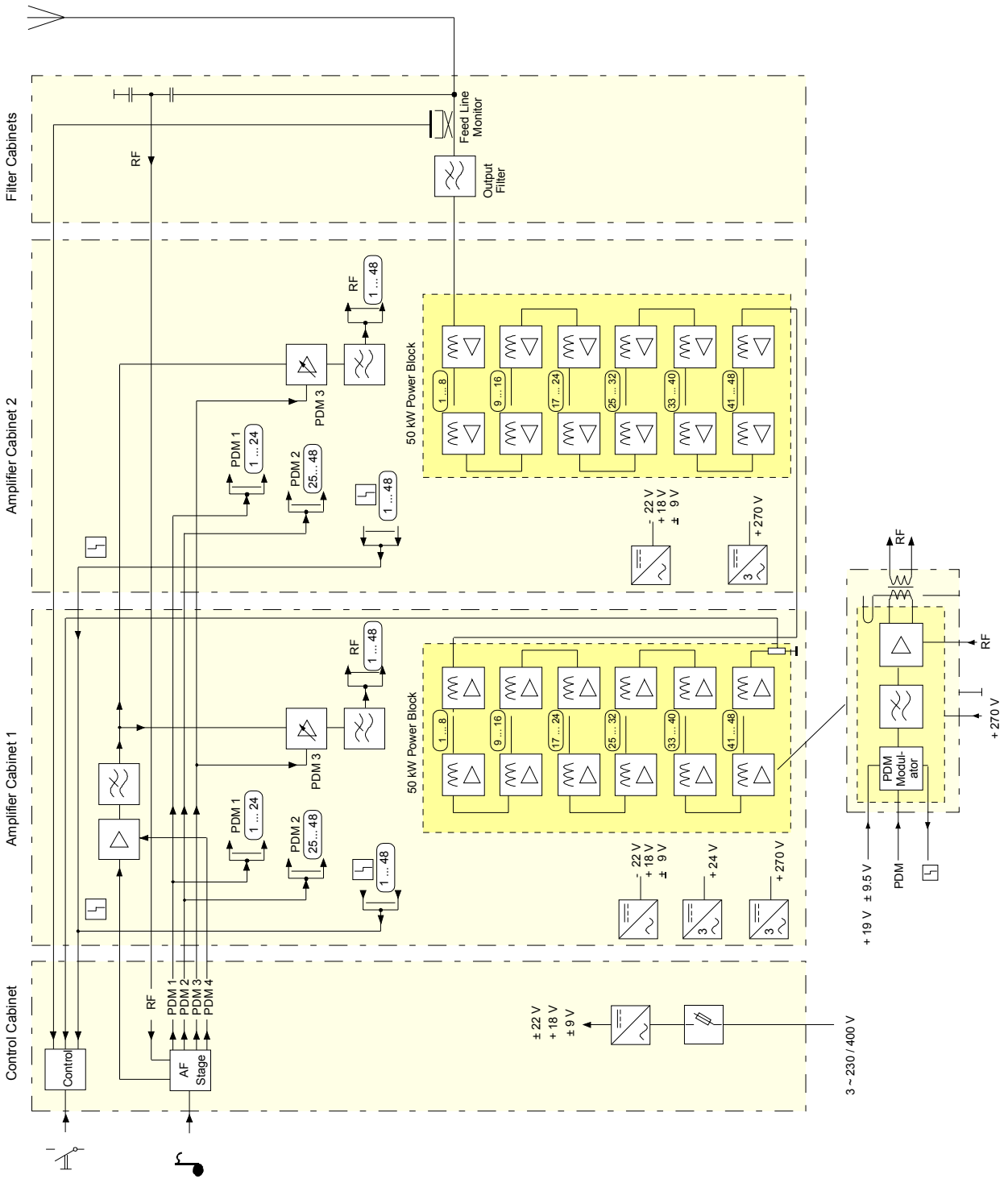

Fig. 2 - 1: Simplifier Block Schematic of the Transmitter

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3 TECHNICAL DATA

Configuration	96 amplifier modules, each incorporating an RF amplifier and a PDM modulation amplifier, 2 drive module2 of the same type, 1 RF predriver
Rated power	100 kW
Output power (carrier)	Selectable P1 or P2 P1 adjustable: 50 kW to 100 kW; P2 adjustable: 25 kW to 50 kW
Frequency Range	525 kHz … 1705 kHz The transmitter is tuned to the operating frequency of 954 kHz
Operating modes	AM (A3E) DAM (X3E)
RF output	
Connector	3 1/8” EIA
Load impedance	50 Ω unbalanced
VSWR	s ≤ 1.5
Modulation type	Amplitude modulated by means of pulse duration modulation
AF frequency response	± 0.5dB: 30 Hz ... 10 kHz (band limiting filters switched off)
AF range	30 Hz ... 10 kHz Two band limiting filters selectable: 60 Hz ... 4500 Hz 60 Hz ... 7000 Hz
AF harmonic distortion	≤ 1% at m = 0.8
Modulation capability	100% continuous
Carrier shift (amplitude drop)	≤ 3%
Harmonics	CCIR 329-6 or better (≤ 50 mW)
Spurious emissions	CCIR 329-6 or better (≤ 50 mW)
Unweighted s/n ratio	≥ 60 dB, referred to 100 % modulation
Frequency stability	Deviation ≤ 5 Hz in 3 months
AF input impedance	600 Ω balanced (2000 Ω selectable by means of soldered jumper) Adjustable from - 10 ... + 10 dBm for 100 % modulation Coarse settings by means of switch, fine settings by potentiometer

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Power Supply	
Mains input	Three-phase 380/400 V; TN-S mains configuration
Mains frequency	50 Hz
Voltage fluctuations	≤ ±5% (performance values not affected) ≤ ±10% (slight reduction in performance values)
Power factor	≥ 0.9
Power consumption	≤ 120 kW at m = 0; ≤ 180 kW at m = 1
Efficiency	≥ 84%
Metering	Pointer instruments for summed current and voltage of the amplifier blocks. Cross-point meter for output power and mismatch, modulation meter, phase meter. Provision made for the connection of a second external cross-point meter.
Control	
Local mode	Full power P1 / OFF, reduced power P2 AM / DAM On-/Off switching and switchover of two LP filters, 4 kHz / 7 kHz Numerous status indications signaled by LEDs Local/Remote switchover PDM enable / inhibit Inhibiting the local mode keys by means of a slide switch (protection against unintentional touching) Clear button for fault indications
Remote mode	Command inputs (the same as in local mode except for local/remote switchover and PDM ON/OFF) by contacts referred to + 24 V given out by the transmitter when under remote control. Output of indications via floating contacts.
Environmental conditions	
Temperature	-10° C … 45° C
Relative humidity	max. 95% (at max. 26° C)
Installation height	max. 2000 m above MSL
Cooling	Air cooled
Dimensions	1800 x 1000 x 2000 mm (W x D x H) cabinet dimensions 1800 x 1080 x 2000 mm (W x D x H) overall with doors and locks

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4 OPERATION

(see also "Pushbutton Keys, Slide Switches and Meters " in Annex 1)

4.1 Before Normal Transmitter On/Off Switching

The transmitter is connected to the mains supply by engaging the main switch in the lower part of the control cabinet. As confirmation that mains voltage is present, LEDs in the control panel, signaling the current status of the transmitter, turn on after about 4 s. The main switch is not intended for normal transmitter on/off switching and cannot be remotely controlled.

4.2 Local / Remote Switchover

The transmitter can be controlled either locally via the control panel pushbutton keys or by supervisory equipment when set to remote mode. Switching between local and remote is by means of keys S1 and S2 in the control panel. The mode selected is indicated by the LED in the respective key and stored in a bistable relay.

In order that commands can be given by the keys of the control panel in local operation, slide switch S15 must be placed in the left position and LED H14 must be off. This LED signals whether the control panel keys are enabled or blocked. The keys are blocked when H14 is on.

In the following, transmitter operation in local mode is described. Nearly all commands can also be given by supervisory equipment when the transmitter is switched to remote.

The selected operating state and parameters are stored in bistable relays, indicated by the LEDs in the respective keys and passed to supervisory equipment through floating contacts.

4.3 Transmitter Switch-On in Normal Operation

The first step for normal operation is the selection of the output power: Power "P1" is selected with key S5 and power "P2" is selected with key S4. When power is selected, the auxiliary contactor, and after a delay time, the main contactor are switched on and the filter capacitors of the predriver, drivers and amplifier modules are charged. The LED in the respective key lights up to confirm that the command has been stored. Furthermore LED H16 " **I** " lights up to indicate that the main contactor in the power supply is engaged. Meter P20 must display an operating voltage of approx. 270 V for both amplifier cabinets (selection is by means of rotary switch S1).

The transmitter is finally switched on by pressing key S7 " **I** PDM" which releases the pulses (in case this command was not previously stored). Pulse release is signaled by LED H15 "PDM". The output power and antenna mismatch can be read from the cross-point meter P10. Meter P30 displays the rectifier current of both amplifier cabinets (selection is by means of rotary switch S2). Meter P40 displays the phase of the antenna tuning.

4.4 Normal Transmitter Switch-Off

Under normal operating conditions, the transmitter is switched off by pressing key S3 "**O**" which gives the "OFF" command. This action blocks the PDM pulses and the main contactor in the power supply is disengaged.

4.5 PDM On / PDM Off

These commands are issued by pressing the keys S6 "**O** PDM" for pulse blocking and S7 " **I** PDM" for pulse release. The transmitter does not deliver output power when the pulses are blocked, however, the main contactor is still engaged.

.

4.6 Switchover between AM and DAM

AM and DAM switch commands are given by keys S8 for AM operation and S9 for DAM operation. The display in cross-point meter P10 shows that the carrier is modulation independent in AM operation and modulation dependent in DAM operation.

4.7 Limiting the AF Frequency Response

A low-pass filter can be enabled or inhibited using keys S11 "**I** ≋" and S10 "**O** ≋" respectively. Keys S12 "≋ 1" and S13 "≋ 2" are used to select between two fixed limiting frequencies. These frequencies may be found in the section "Technical Data".

5. SETTING THE OPERATING PARAMETERS

5.1 Matching the Input Level

The modulation factor "m" can be read at the modulation meter P50. To set "m", the studio signal is connected to the AF input, slide switch S4 is placed in the left position "AF out" and the modulation factor is adjusted to the desired value using the coarse rotary switch (+ 5...-10 dBu) and the fine tuning potentiometer (+ 5...0 dBu) adjacent to the AF input connector X1 on the control panel.

5.2 Setting the Output Power "P1" and "P2"

To set the desired output power given when the command keys S5 "P1" and S4 "P2" are pressed, open the control panel door when the transmitter is switched on and adjust the power P2 using potentiometer R8 and power P1 using potentiometer R6 on the control board (refer to Section 14: **Preparing for Operation**, sub-section 14.4). The factory setting is P1: 100 kW and P2: 50 kW.

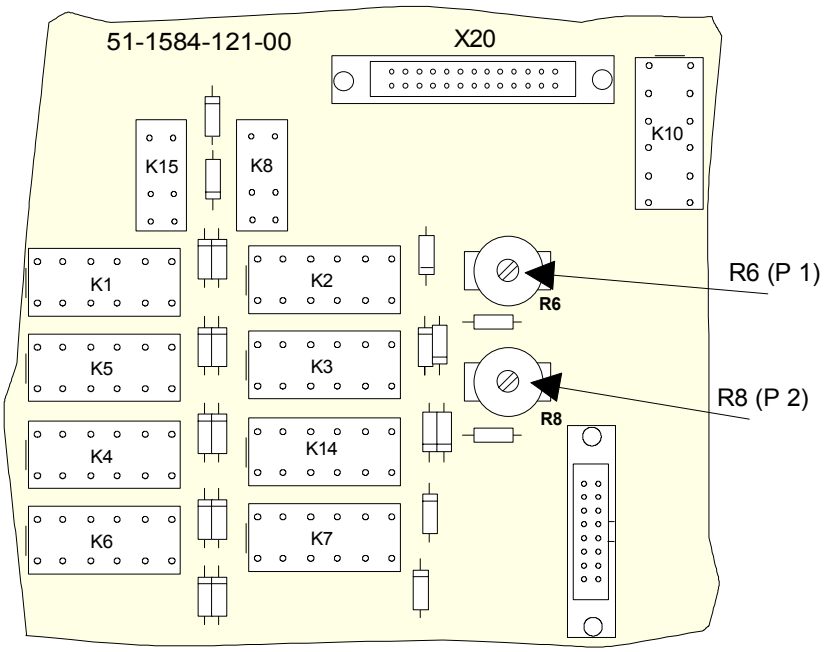

Fig. 5.2 - 1: Location of Potentiometers R6 and R8 on the Control Board

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6. FUNCTIONAL DESCRIPTION

6.1 Basic Principles

6.1.1 Comparison between Dynamic-Controlled Amplitude Modulation (DAM) and Amplitude Modulation (AM)

In the medium wave band the transmitted signal is usually amplitude modulated (AM). The spectrum consists of a constant carrier U_c and two sidebands U_{s-} and U_{s+} which contain the information. The carrier conveys no intelligence but requires the greater part of the radiated energy.

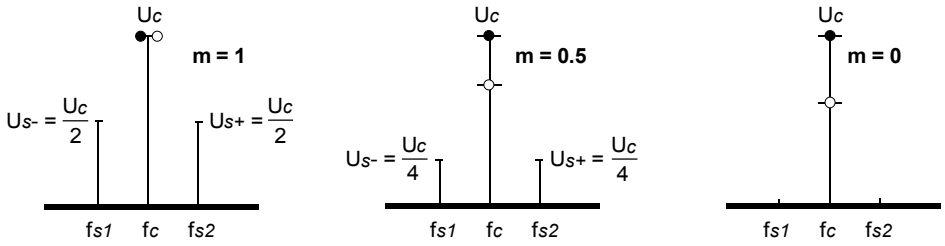

Fig. 6.1.1 - 1: Spectrum without (•) and with DAM (o)

In Dynamic-controlled Amplitude Modulation (DAM) the carrier is controlled by the dynamics of the AF signal. This means that if the modulation is small or zero, the amplitude of the carrier is reduced to a residual value and only with increasing modulation swing is the amplitude of the carrier raised to the nominal value. The radiated power in the sidebands is the same for AM and DAM at equal modulation, however, the carrier power is on average lower in DAM operation.

Fig. 6.1.1-2 shows the relationship between the modulation swing "u" and the relative carrier amplitude in AM and DAM. In DAM operation, with a modulation swing of $0 \leq u \leq 0.45$, the carrier amplitude is reduced to a constant 60% (carrier residual value). The carrier power is 36% of the power in AM operation.

Due to "carrier offset" the characteristic curve begins to rise from u = 0.45 onwards. The carrier offset of 15% is selected to prevent high modulation factors at small modulation swing and to prevent the occurrence of overmodulation. This situation would result when the AF level rises faster than the carrier amplitude. On the other hand, a fast rising carrier amplitude would result in additional modulation with a corresponding increase in out-of-band emissions - this must be prevented. Experience has shown that optimal conditions are achieved with a carrier rising edge time constant of 0.2 ms and a carrier falling edge time constant of 100 ms.

As opposed to AM, this type of carrier control, during programme modulation, saves more than a third of the radiated power without affecting the sidebands.

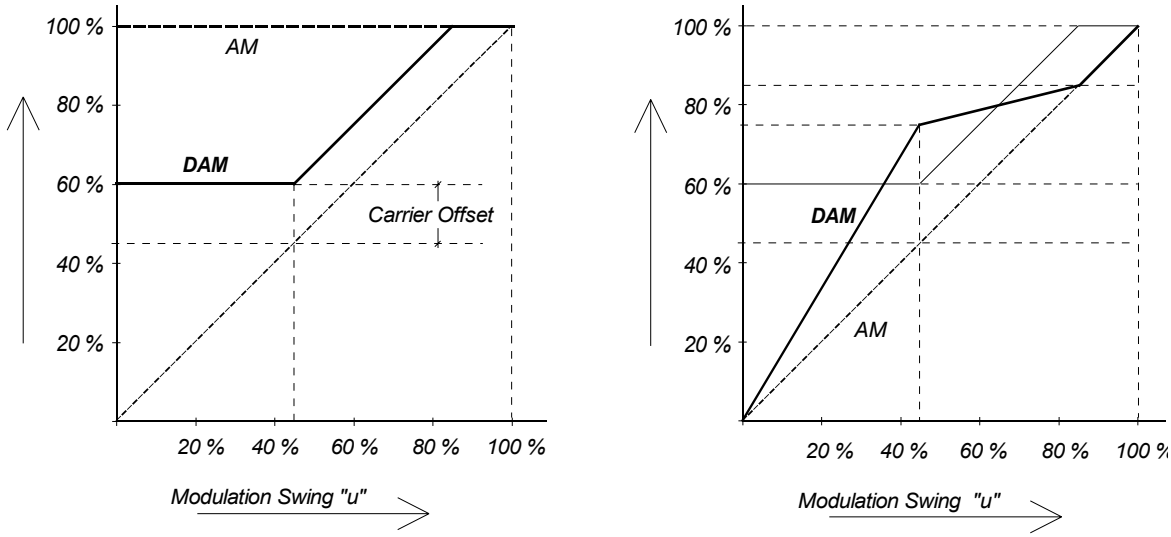

Fig. 6.1.1 - 2: DAM Curves for Carrier Amplitude vs. Modulation Swing
and Modulation Factor vs. Modulation Swing

The above described control of carrier amplitude in the transmitter takes place in the AF Stage A1200 of the control section. Here, the AF input signal is superimposed with a dc voltage corresponding to the carrier value. In AM this voltage is a constant and in DAM it depends on the dynamics of the AF which, however, never drops below a fixed value representing the residual carrier.

6.1.2 Signal Amplification by Means of PDM

In Pulse Duration Modulation (PDM) an amplifier is employed which operates as a switching device, thereby achieving high efficiency.

6.1.3 PDM Method

The PDM method involves changing the pulse width of a square wave signal of constant frequency as a function of the AF voltage. The relationship between the AF voltage and the pulse width is linear. The amplified AF voltage which corresponds to the arithmetic mean of the PDM signal can be recovered from this signal by a simple low-pass filter.

The amplified AF signal serves as the drive voltage for the actual high frequency amplifier.

6.1.4 Generating the PDM Pulses

The PDM pulses are generated by the comparison of an input voltage U_{in} (either pure dc - see RF Signal Conditioning or the processed AF input voltage - see AF-PDM Processing) and a triangular wave form U_{tr} in a comparator. As long as $U_{in} > U_{tr}$, the comparator delivers a voltage U_{PDM} which is used to drive switching transistor T1 in the PDM amplifier. The downstream low-pass filter passes only the low frequency and dc components of the PDM square-wave signal.

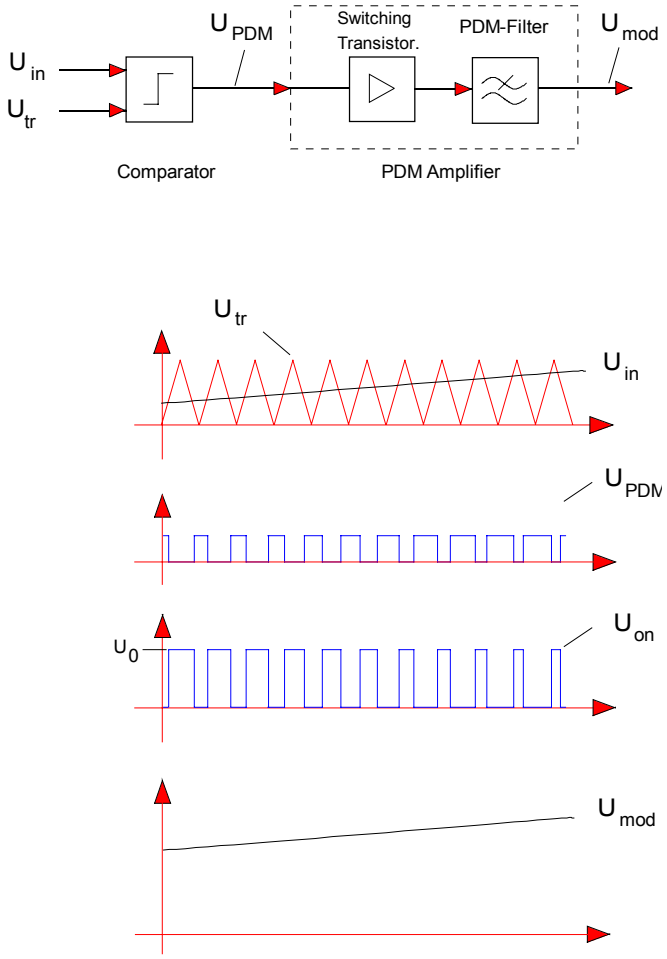

Fig. 6.1.4 - 1: Principle of PDM Amplification

6.1.5 Amplification and Filtering

Fig. 6.1.4 - 1 above, shows the basic principle of PDM amplification with the associated signal forms. The PDM amplifier (see Fig. 6.1.6 - 1) consists essentially of the switching transistor T1, commutating diode D1 and the downstream PDM filter which suppresses the switching frequency components of the on-state voltage U_{on} of T1.

The output voltage U_{mod} of the PDM amplifier drives the downstream RF power amplifier (R_{load}).

6.1.6 Operation of the PDM Amplifier

Switching transistor T1 is driven by the PDM pulses. When the transistor conducts, the current I_{T1} flows through the load, the filter and T1 to ground. During this time the voltage at point U_{on} is the on-state voltage of the transistor. When T1 is blocked the current I_{D1}, driven by the stored magnetic energy in the filter coils, flows through the load, the filter and diode D1. During this time the voltage at point U_{on} is the operating voltage U_0 plus the forward voltage of D1.

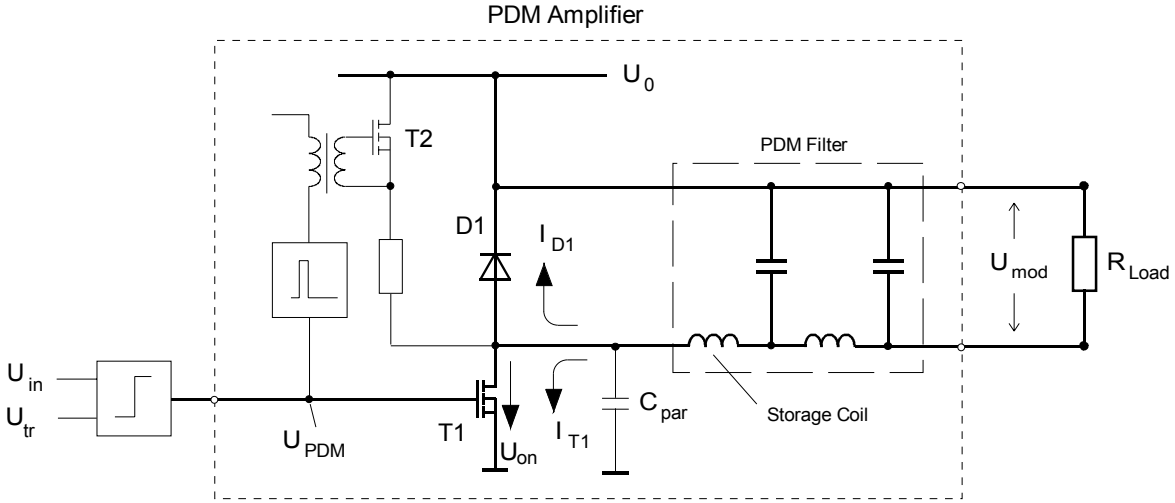

Fig. 6.1.6 - 1: Operating Principle of the PDM Amplifier

The mean value of the storage coil current flows through the load, while the switching frequency current components are suppressed by the filter. The magnitude of the current through the load and thus the value of U_{mod} is dependent on the switch-on time of T1. The value of U_{mod} is greater the longer T1 conducts.

Essentially, the relationship between the switch-on time of transistor T1 and the current through the load is linear.

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Due to the parasitic capacitance C_{par} between T1 and D1 formed by the circuit elements, the relationship between the switch-on time of T1 and the current through the load is non-linear. This may be explained as follows:

At the time T1 conducts, C_{par} previously charged to the operating voltage U_0 is discharged through T1. The discharging time is relatively fast due to the low internal impedance of T1. At the time T1 is in the off-state (high impedance), C_{par} is charged to the operating voltage U_0 by the current generated by the magnetic energy stored in the filter coil. The switching process is slower the smaller the current through the filter coils so that at low duty factors the rising edge of the pulses are deformed.

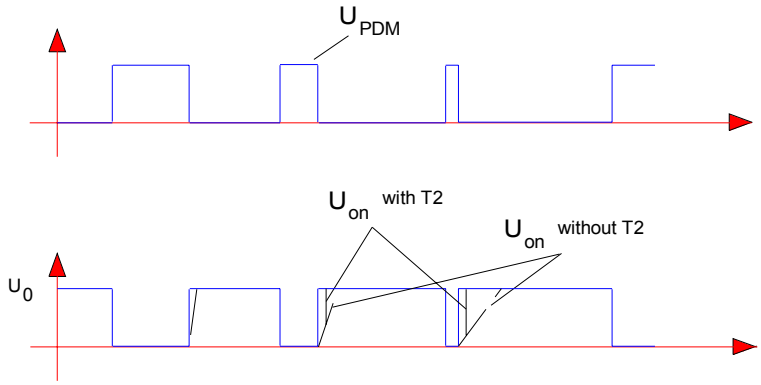

Fig. 6.1.6 - 2: Relationship between Operating Voltage U_0 and Duty Factor

This deformation manifests itself as a value $U_{mod} = U_R$ which "bends" the linear characteristic curve.

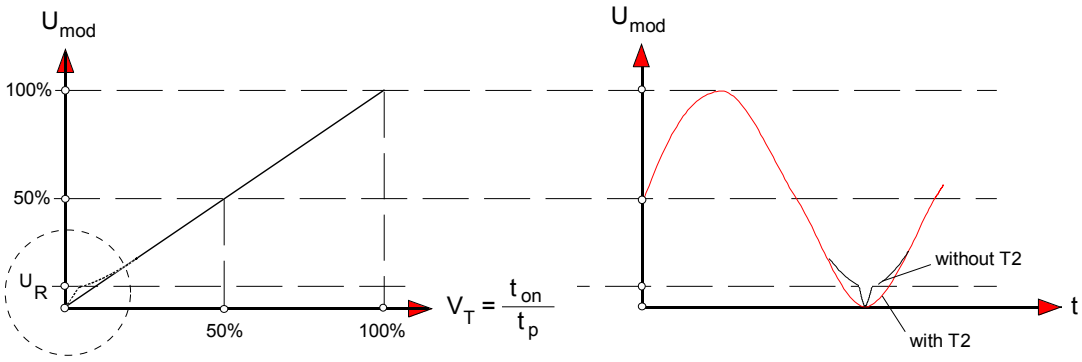

Fig. 6.1.6 - 3: Bending of the Characteristic Curve due to the Parasitic Capacitance C_{par}

6.1.7 Purpose of the Discharge Switch T2

In order to linearize the curve, transistor T2 located parallel to D1 conducts for a short period after transistor T1 blocks, thereby discharging the parasitic capacitance C_{par}. T2 is driven by short square-wave pulses derived from the PDM signal.

6.1.8 RF Power Amplifier

The RF power amplifier consists basically of four MOSFET switches operating pair-wise in push-pull mode (H-bridge). The gates of the MOSFETs are driven by four secondary windings of a transformer, whereby gate pairs are driven in phase opposition so that one of the two in series connected MOSFETs turns on. The control voltage for the gates is the RF driver voltage U_{RF}. The voltage U_{mod} delivered by the PDM amplifier is switched through by the MOSFETs at the radio frequency.

The bridge output voltage U_{Br} is thus a square-wave oscillation with a frequency corresponding to the that of the control voltage U_{RF} and an amplitude corresponding to that of the operating voltage U_{mod}.

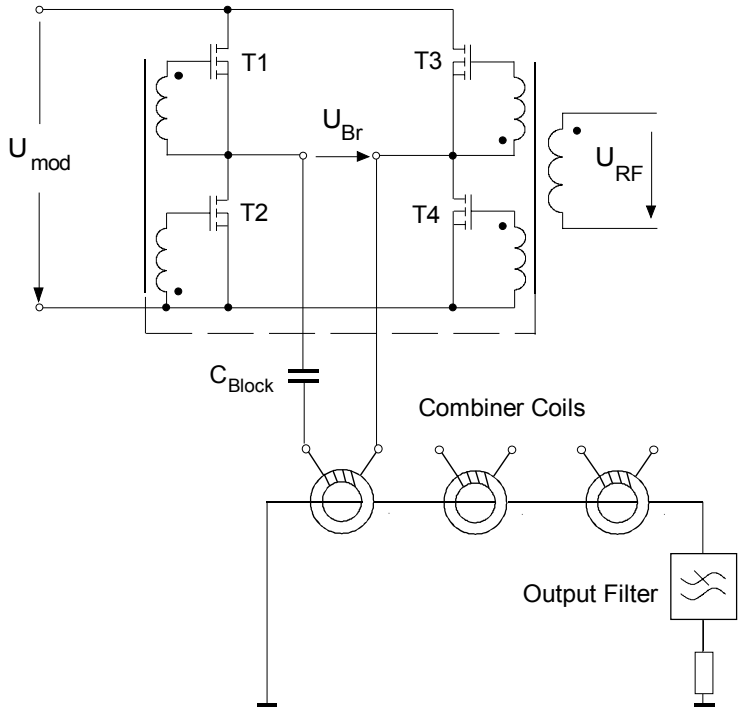

Fig. 6.1.8 - 1: Operating Principle of the RF Power Amplifier

The square-wave amplitude modulated output U_{Br} is coupled out by means of a transformer circuit (combiner coil). The bypass capacitor ahead of the transformer prevents a dc current from flowing through the transformer and the cross arm of the H-bridge under asymmetric conditions.

6.1.9 Tuning the Load Circuit for the RF Power Amplifier

The output (load) circuit connected to the secondary of the transformer (combiner coil) is tuned so that only the current of the RF fundamental wave is coupled out.

In the following, consideration is given to the switching characteristics of the H-bridge under three possible conditions - real, slightly capacitive and slightly inductive load circuits. It will be shown that a slightly inductive circuit gives the lowest switching losses in the MOSFETs.

The symmetry of the H-bridge allows an equivalent circuit to be considered, consisting of half the bridge, enabling the switching characteristics to be studied. As a simplification, the output filter and the combiner are represented by a wave trap consisting of C_{eq}, L_{eq} and the load R_{load}.

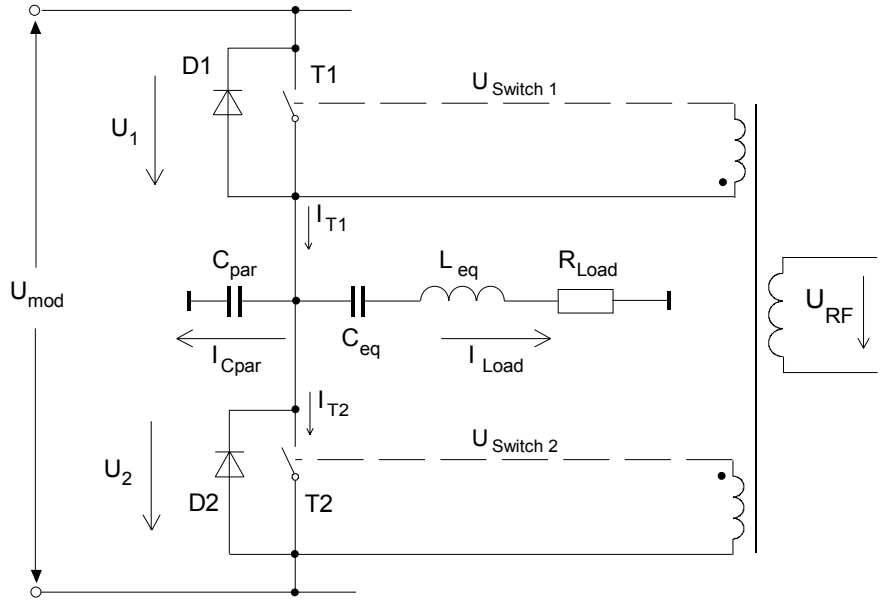

Fig. 6.1.9 - 1: Equivalent Circuit of the H-Bridge to Study Switching Characteristics

The MOSFETs are represented as switches with diodes connected in parallel. All parasitic capacitance's are combined in C_{par}.

In order to prevent switch-on overlapping and consequently short circuit currents, the switches must be driven so that during the switchover process, a time interval is introduced in which all MOSFETs are in the non-conducting state. This is achieved with a nearly sinusoidal drive voltage, which, close to the zero crossover, provides an insufficient gate voltage to turn on the MOSFETs. During this time, the load current can only flow through the diodes D1, D2 or C_{par}.

6.1.10 Switching Characteristics with a Real Tuned Load Circuit

The timing diagrams are shown in Fig. 6.1.10 - 1. No phase shift exists between the fundamental wave of the current i_{Load} and the fundamental wave of the voltage $U_{switch\ 1,\ 2}$. The current zero crossover point occurs at a time when both switches are in a high impedance state.

At t_0 the load current i_{Load} rises both switches are in a high impedance state and the voltage U_2 drops slowly. As long as its value is above the negative value of the on-state voltage of diode D2 the load current reverse charges the parasitic capacitance $i_{Cpar} = -i_{load}$. Thereafter the current i_{D2} flows through diode D2 and the voltage U_2 takes on the value of the on-state voltage which is small compared to the operating voltage U_0.

At t_{11} switch T1 is in a low impedance state, the current now flows through T1 and U_2 takes on the value of the operating voltage minus the value of the voltage drop across the switch. Since the voltage at T1, during the switching process, does not drop suddenly, switching losses occur. These increase because the charge at C_{par} is suddenly reversed and the charge reversing current also flows through the switch.

At t_{12} switch T1 is again in a high impedance state. To begin with $i_{Load} = i_{Cpar}$. Only when U_2 drops to about the negative value of the on-state voltage of diode D2 does current flow this diode. The charge reversing current of C_{par} is taken up in the load circuit and additional switching losses do not occur. At $t/_2$ the current changes direction and the process is repeated for switch T2.

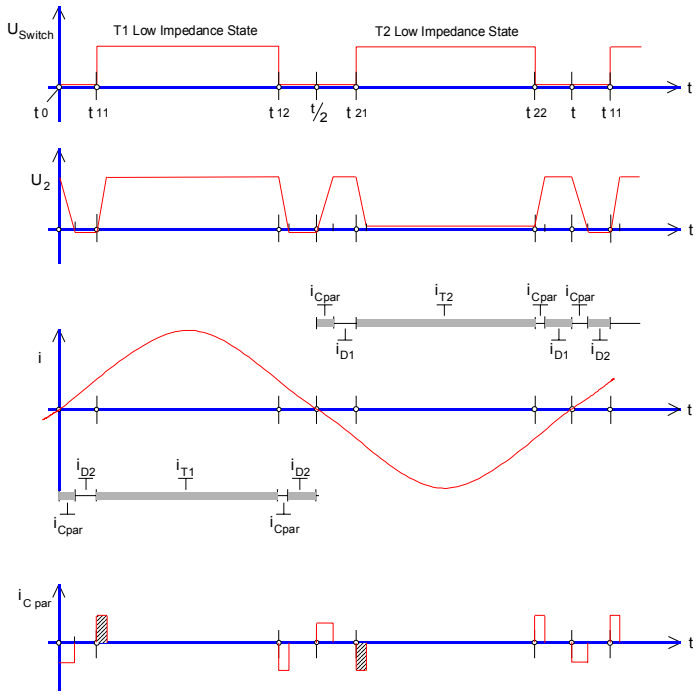

Fig. 6.1.10 - 1: Timing Diagrams with a Real Tuned Load Circuit

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6.1.11 Switching Characteristics with a Capacitively Tuned Load Circuit

The timing diagrams are shown in Fig. 6.1.11 - 1. The fundamental wave of the current leads the fundamental wave of the voltage $U_{switch\ 1,\ 2}$.

At t_0 the current i_{Load} is positive and flows through diode D2. The voltage U_2 is negative and has the magnitude of the diode forward voltage.

At t_{11} switch T1 is in a low impedance state, the current now flows through this switch and the voltage U_2 takes on the value of the operating voltage minus the value of the voltage drop across the switch. Since the voltage at T1, during the switching process, does not drop suddenly, switching losses occur. These increase because the charge at C_{par} is suddenly reversed and the charge reversing current also flows through the switch T1.

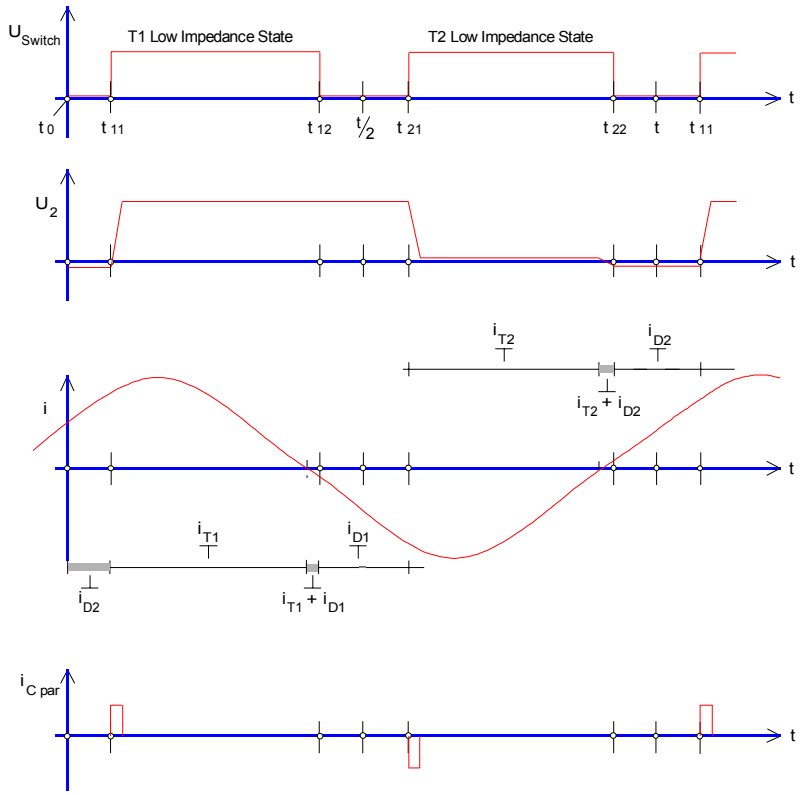

Fig. 6.1.11 - 1: Timing Diagrams with a Capacitively Tuned Load Circuit

Shortly before t_{12} the current changes direction and is distributed, depending on the internal impedance of switch T1 and the voltage drop across diode D1, through the switch and diode.

At t_{12} switch T1 is in a high impedance state and the current flows only through diode D1. This switching process takes place without any appreciable change of the voltage at the switch, thus switching losses do not occur and the parasitic capacitance C_{par} does not undergo a sudden charge reversal. At t_{21} switch T2 is in the low impedance state and the above described process for T1 is repeated for T2.

6.1.12 Switching Characteristics with a Inductively Tuned Load Circuit

The timing diagrams are shown in Fig. 6.1.12 - 1. The fundamental wave of the current lags the fundamental wave of the voltage $U_{switch\ 1,\ 2}$. At t_0 both switches are in a high impedance state and a current flows through the diode D1. At t_{11} switch T1 is in a low impedance state. This switching process takes place without any appreciable change of the voltage at the switch since the current is already flowing through the parallel connected diode D1. Switching losses do not occur. At t_{12} switch T1 is again in a high impedance state and the current now flows through the diode D2. The parasitic capacitance C_{par} is charged reversed by the load current. At t_{21} switch T2 is in a low impedance state. Also this switching process takes place without any appreciable change of the voltage at the switch since the current is already flowing through the parallel connected diode D2. Switching losses do not occur.

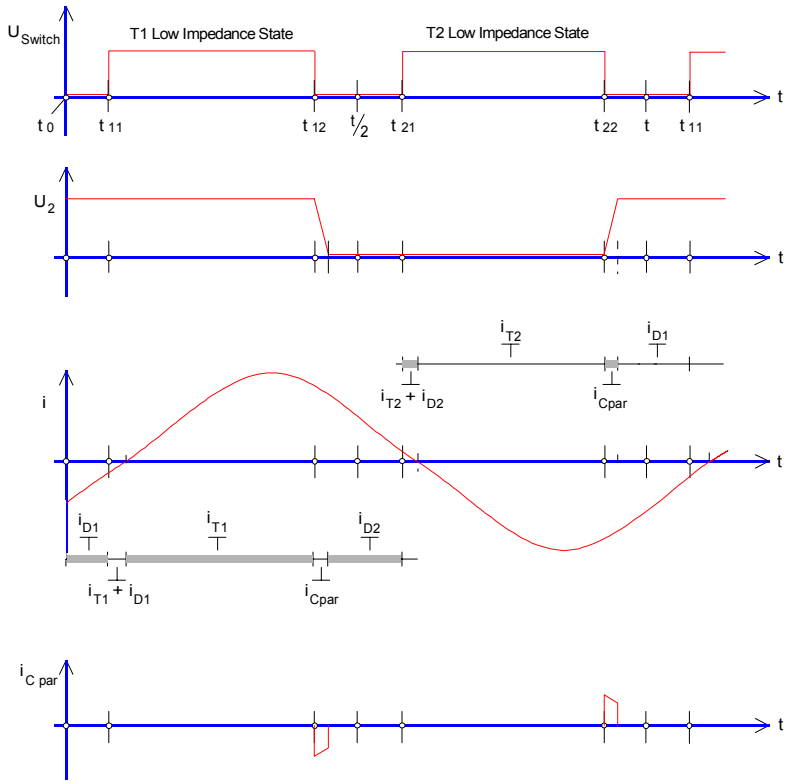

Fig. 6.1.12 - 1: Timing Diagrams with an Inductively Tuned Load Circuit

6.1.13 Comparison of the Switching Characteristics of the Variously Tuned Load Circuits

A comparison of the switching characteristics shows that with an inductively tuned load circuit no direct switching losses occur in the MOSFETs since at the point of switching, the reverse charging of the parasitic capacitance C_{par} has already taken place through the load current. Therefore the only losses remaining are those incurred during switching under voltage loads and the on-state loss of the diodes which form an integral part of the MOSFETs. Since the inductive tuning involves the lowest losses it is selected to achieve high RF amplifier efficiency.

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7. FUNCTIONAL GROUPS

7.1 AF-PDM Signal Path

The balanced AF signal is fed to the input stage [1], converted into an unbalanced signal and then passed to the downstream level control [2] where the amplitude is matched to the desired modulation factor. The filter circuits [3] and [4] limit the bandwidth of the AF signal.

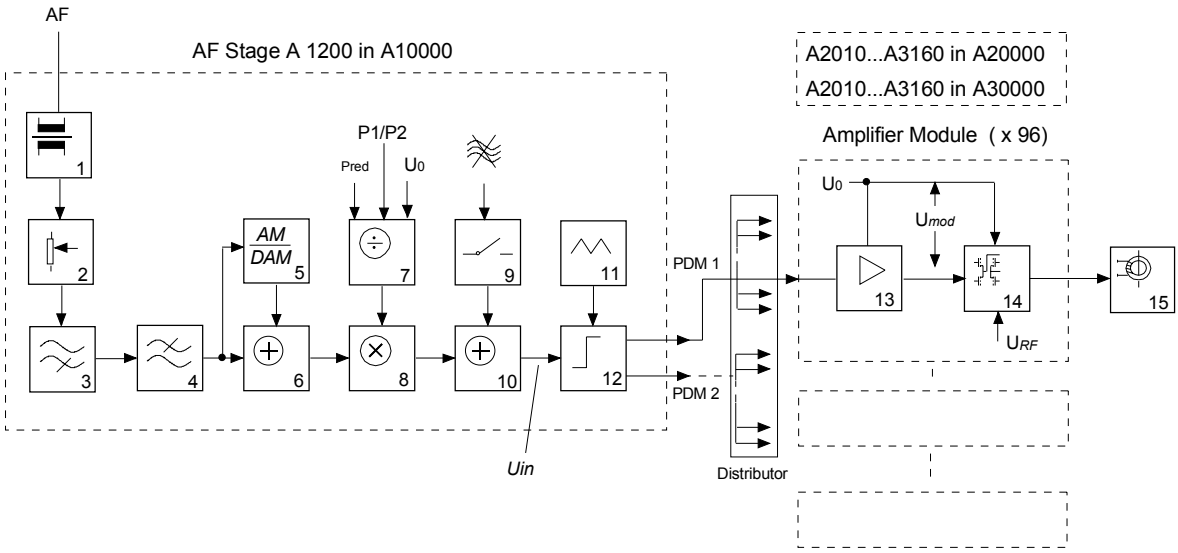

Fig. 7.1 - 1: AF-PDM Signal Path

[1]	Input Stage
[2]	AF Level Control
[3]	High-pass Filter
[4]	Low-pass Filter
[5]	Carrier Control
[6]	Adder Stage
[7]	Compensation
[8]	Envelope Weighting
[9]	Pulse Blocking
[10]	Pulse Inhibit/Enable Circuit
[11]	Triangular Wave Form Generator
[12]	Comparator Circuit
[13]	PDM Amplifier
[14]	RF Power Amplifier
[15]	Combiner Coil

In the adder stage [6] a dc voltage, which determines the magnitude of the carrier value, is superimposed on the AF signal. In AM operation, the dc component is constant, while in DAM it is a function of the dynamics of the AF signal and does not drop below a set value with respect to the residual carrier. The output of this stage forms the envelope of the transmitter output signal.

The multiplier [8] weights the envelope voltage with a value which determines the output power of the transmitter.

In the comparator stages [12], the envelope voltage is compared with a triangular wave form. The output signals are two PDM pulse streams in phase opposition ("PDM 1" and "PDM 2"), each driving one half of the PDM amplifier [13] in the power modules. This form of phase shifted drive serves to provide an additional suppression of the switching frequency components in each pair of switching amplifiers.

7.2 Conditioning the AF Signal

The AF signal is applied through connector X11 of the AF stage and is routed through X12 and the patch plug on the front of the control panel to the balanced input X13. The input level for 50% modulation must be between -10 dB and +10 dB.

Input Stage [1]: This stage has a floating input (here pins X1/1-2 and X2/1-2 as well as X3/1-2 and X8/1-2 on the pc board are jumpered). The input impedance is 600 Ω and can be varied between 600 Ω and 2 kΩ by changing the value of resistor R26. Input transformer T1 may be bypassed by resoldering the jumpered pins X1/2-3 and X2/2-3 as well as X3/2-3 and X8/2-3. The input is then balanced to ground and the input impedance is fixed at 600 Ω. The downstream amplifiers N1...N3 function as balancing amplifiers. Balancing alignment is possible using resistor R16, while diodes V1...V6 protect against input signals which are too high.

AF Level Control [2]: The AF level control is capable of continuously adjusting the AF level in a range of 20 dB by means of potentiometer R21 and switch S1 and thus match the AF level to the desired modulation factor. Amplifier N4 decouples the level control from the following filter circuit.

High-pass Filter [3]: This filter determines the lower frequency limit and is formed by amplifiers N5 and N6. The filter can be bypassed by resoldering jumpers X9/2-3 and X24/2-3.

Low-pass Filter [4]: This filter determines the upper frequency limit and comprises low-pass filters N38 to N40 and N41 to N43 respectively. It can be switched between two limiting frequencies 4.5 and 6.75 kHz (-3 dB) via the control board and relay K1.

Carrier Control [5]: This circuit prepares the signal which is superimposed on the AF in the adder stage. In AM operation, the carrier voltage is a constant, while in DAM operation the carrier voltage is a function of the AF peak value. During AM operation the contact of relay K3 is open and transistor V53 delivers, independent of the modulation signal, a constant voltage corresponding to the maximum carrier value occurring in DAM operation.

In DAM operation, amplifier N7 couples out the AF which is then inverted in amplifier N8 and rectified by diodes V50 and V51 and applied to emitter follower V52. The parallel connected emitter follower V53 prevents the common emitter voltage from dropping below a fixed voltage, set with potentiometer R60, which represents the residual carrier value. The voltage generated in this manner corresponds to the carrier value without carrier offset. The carrier offset is added to the carrier value in amplifier N9 and is determined by R65.

Adder Stage [6]: In the adder stage N10, a dc voltage (dependent on the carrier value) is superimposed on the AF signal. The output of this stage forms the envelope of the transmitter output signal.

Compensation [7]: The compensation voltage is derived in divider N13 from a reference dc voltage and the divided-down operating voltage U_0 (270 V) for the amplifier modules. Since U_0 is proportional to the mains supply, the effects of mains fluctuations are taken into account through the amplitude of the compensation voltage, the amplitude of the envelope signal and thus in effect by the duty factor of the pulse duration modulated AF signal. Furthermore, the hum voltage component of U_0 which would cause unwanted modulation in the amplifier modules is also compensated.

Envelope Weighting [8]: The envelope signal at input 2 of multiplier N12 is multiplied with a compensation voltage applied at input 6. As a consequence, the amplitude of the dc component representing the carrier value and the amplitude of the ac component representing the AF are weighted with the same factor. The amplitude of the envelope signal, set in this manner, controls the output power of the transmitter.

Pulse Inhibit/Enable Circuit [10]: By applying a dc voltage at pin 3 of amplifier N37 the envelope signal fed to the comparators can be shifted in a range of voltages so that the comparators no longer switch. The amplifier N15 provides for fast pulse blocking and relatively slow pulse release. When the transmitter is switched on it is therefore possible to enable the pulses for all amplifier modules simultaneously, and in case of a fault, to inhibit the pulses simultaneously.

Triangular Wave Form Generator [11]: The generator is formed by transistors V167 and V168. The transistors are driven by transistor V169 with a 72 kHz signal derived from the frequency division of a 2.304 MHz crystal. While capacitor C167 is continuously discharged with a constant current through V168 it is periodically charged with double the constant current through V167. The triangular voltage at C167 is made symmetric by feedback through V170. With the aid of the negative feedback circuit comprising transistors V171 and V172, two 180° phase shifted triangular-wave signals are produced which are passed through emitter followers V173 and V174 and made available at low impedance to the comparator circuit.

Comparator Circuit [12]: Comparator circuits N20 and N21 generate two PDM signals phase shifted by 180°. This occurs by comparing the weighted envelope voltage with two triangular wave forms in phase opposition. The output signals are square waves with variable duty factor. PDM enable occurs with a 0 V signal at X15/6. The voltages "PDM 1" and "PDM 2" at the outputs of the comparator stages [12] are passed via distributor boards to the PDM inputs X1/5 of the amplifier modules.

The PDM amplifier [13] in the amplifier module comprises transistors V5 and V6 connected in parallel which function as the PDM switch, transistor V4 functioning as the discharge switch, commutating diode V3 and the PDM filter consisting of inductor L1, L2 and capacitors C8...C14 and C16..C24. The trap circuit for the switching frequency is formed by L2 parallel to C25 and C26.

The output voltage of the PDM amplifier which drops across the filter output capacitance provides the operating voltage for the **RF power amplifier [14]** formed by transistors V26...V37. The actual amplitude modulation takes place in the RF switching stage since the magnitude of the operating voltage (i.e., variation in pulse duration) determines the amplitude of the signal delivered by this stage.

7.3 Pulse Processing in the Amplifier Module

The PDM signal applied through X1/5 is decomposed behind gate D4/3 (through which pulse blocking can be initiated by the monitoring circuit internal to the module) into the actual signal to drive the switching amplifier and a further signal used to control the discharge switch.

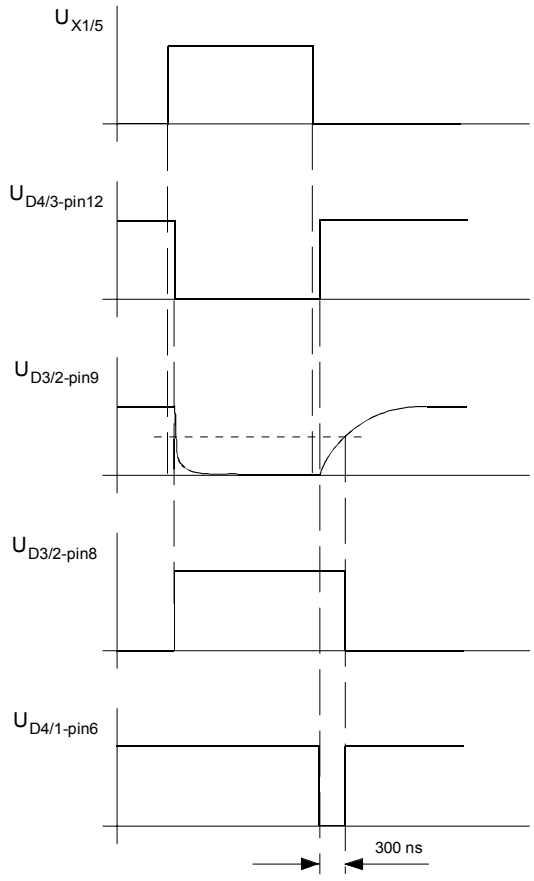

Fig. 7.3 - 1: Pulse Processing in the Amplifier Module

The PDM signal path comprises inverter D4/2 and the drive circuit D6 which drives the parallel connected PDM switching transistors V5 and V6.

In a side path, a pulse sequence is derived from the PDM pulses which drives the discharge switch V4 for about 300 ns after each PDM "switch-off" edge as long as the duty factor of the PDM pulses is smaller than about 45%. The enabling of the pulses, dependent on the duty factor, takes place via pin 3 of gate D4/1.

The PDM pulses are inverted in D4/3 and shaped by means the RC combination R49/C50 and diode V10. The output voltage $U_{D4/1\text{-pin }6}$ is generated by the AND interconnection of the voltages $U_{D3/2\text{-pin }8}$ and $U_{D4/3\text{-pin }12}$ and the subsequent signal inversion in gate D4/1. This output voltage produces a "low" pulse of about 300 ns duration at the "switch-off" edge of the PDM pulse and is passed via driver D5 and transformer T1 to control transistor V4 functioning as a discharge switch.

The turning on of transistor V4 for a short period results in a discharging of the parasitic capacitance of the PDM amplifier and linearizes the amplifier characteristic curve.

The discharge switch is only turned on when a high is present at the output of gate D3/1 and thus also at pin 3 of NAND-gate D4/1. A signal is present at the input of gate D3/1 (functioning as an inverter), which corresponds to the mean of the PDM signal taken from the output of gate D4/2. The mean value is taken from the low-pass R48/C61. If the duty factor is below about 45%, the voltage at the input of gate D3/1 drops to such an extent that a high is present at the output of gate D3/1 and the discharge switch can be driven via gate D4/1.

7.4 Power Supply

The transmitter is connected to mains power by manually engaging main switch [1]. Thereafter, the auxiliary voltages are available at the outputs of the power supplies [9] and the fans in the fan tray unit [2] are switched on. When key P1 or P2 in the control panel is pressed, contactor [4] is switched on and mains power is applied through charging resistors [3] to the main power supply [7]. The charging resistors limit the current to charge the filter capacitors in the amplifier modules, driver and predriver.

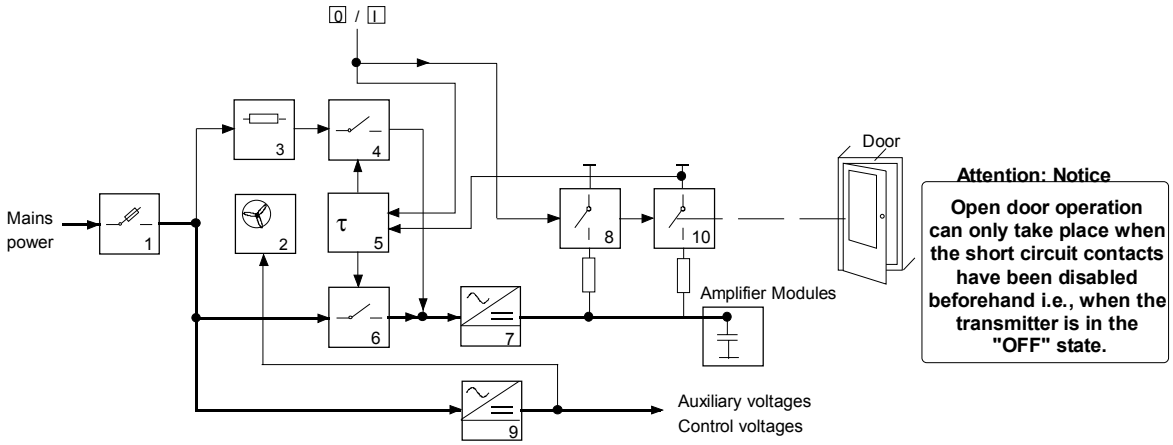

Fig. 7.4 - 1: Block Schematic of the Transmitter Power Supply

[1]	Main switch	[6]	Main contactor
[2]	Fan tray unit	[7]	Main power supply (transformers)
[3]	Charging resistors	[8]	Discharge circuit A 4060 / A 20000
[4]	Contactor	[9]	Auxiliary voltage supplies 1 + 2, 24 V power supplies
[5]	Switch-on Delay Board	[10]	Discharge circuit (short circuit contacts)

Main contactor [6] is engaged after a delay determined by the switch-on delay board [5] via contactor [4]. Thereafter, the rectifier is connected to the power supply and delivers operating voltage to the modules. The discharge circuit [8] is deactivated as long as a switch-on voltage is present at contactor [4]. When the transmitter is switched off, contactor [4] and main contactor [6] drop out and the filter capacitors of the amplifier modules, drivers and predriver are discharged through discharge circuit [8]. A discharge circuit [10] is activated when the door of the amplifier cabinet is opened.

7.5 RF Signal Conditioning

The RF is generated by the synthesizer board [1] – see Section 7.6 for a detailed description. The downstream predriver amplifies the output signal of the synthesizer board to a level sufficient to drive the downstream RF drivers. The RF output signal of the predriver, whose amplitude is determined by the pulse width of the PDM 4 voltage of the AF stage, is passed through series damping circuit 1, consisting of a transformer [6], series resistor [7] and series inductor [10] to the input of the drivers.

The drivers provides the RF power to drive the 2 x 48 amplifier modules. The RF output signal of the driver, whose amplitude is determined by the pulse width of the PDM 3 voltage of the AF stage, is passed to the inputs of the amplifier modules through series damping circuit 2, consisting of a transformer and series resistor as in series damping circuit 1 and series inductor [16] formed by three inductors connected in parallel.

The amplifier modules [13/14], driven in parallel, deliver the RF output power of the transmitter. The amplitude of the output voltage of the amplifier modules is determined by the PDM 1 and PDM 2 voltages and modulated with AF.

The combiner [15] sums the 96 outputs of the amplifier modules by means of a series transformation circuit. The primaries of the 96 individual transformers are connected to the outputs of the amplifier modules while a common secondary is passed through the ring cores of the transformers.

Downstream of the combiner is the output filter which is designed to pass the fundamental of the output voltage while attenuating the harmonics. Behind the filter is a capacitive voltage divider which is used to couple out voltages for the demodulator and test points. In addition a feed line monitor and a grounding switch are located at the output of the filter.

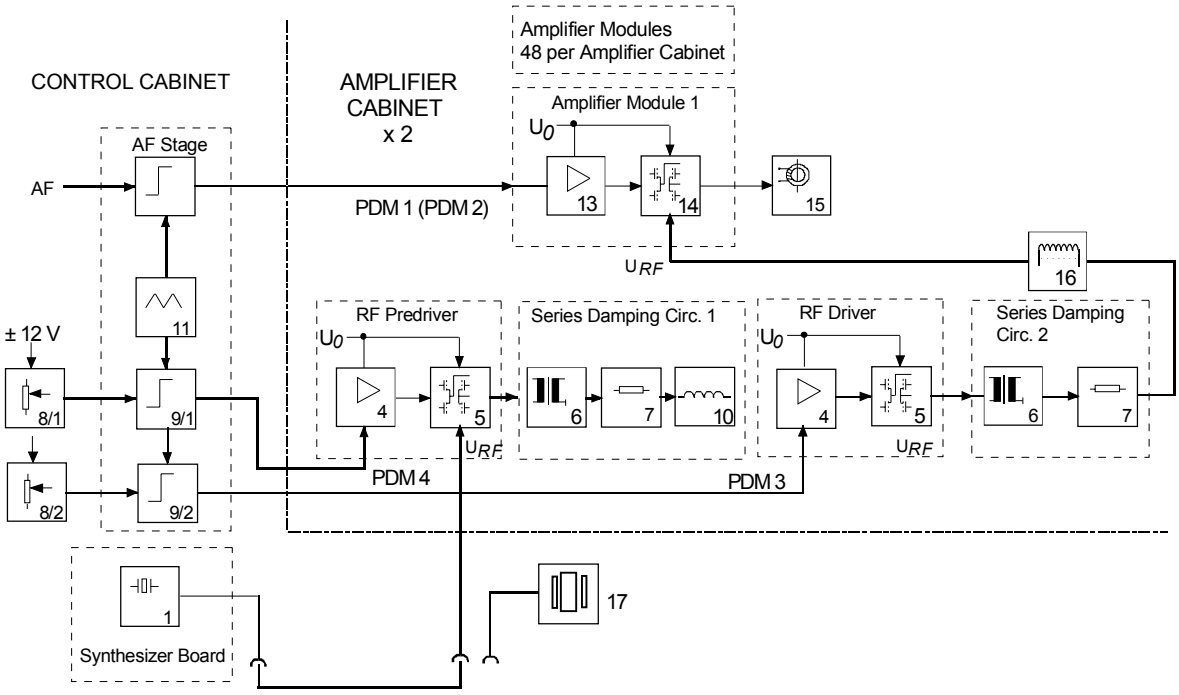

Fig. 7.5 - 1: Signal Path in the Transmitter

[1]	Synthesizer Board	[10]	Series Inductor
[4]	PDM Amplifier	[11]	Triangular-Wave Generator
[5]	RF Power Amplifier	[13]	PDM Amplifier
[6]	Transformer	[14]	RF Power Amplifier
[7]	Series Resistor	[15]	Combiner
[8]	RF Amplitude Setting	[16]	Series Inductor
[9]	Comparator	[17]	External RF Generator

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7.6 Synthesizer Board

Technical Data

Power requirements:	+18 V, ca. 8 mA
	+9 V, ca. 100 mA
	-18 V, ca. 20 mA
Frequency ranges:	85 - 170 x 10 kHz / 95 - 190 x 9 kHz
	85 - 170 x 5 kHz / 95 - 190 x 4.5 kHz
	85 - 190 x 2 kHz
	85 - 190 x 1 kHz
	85 - 170 x 500 Hz
	95 - 190 x 9 kHz/4
	95 - 190 x 9 kHz/8
	95 - 190 x 9 kHz/16
Output voltage:	approx. 2 V_{pp} (square-wave) across 50 Ω
	approx. 1 V_{rms} (sine-wave), only for LW- and MW broadcasts
Temperature range:	-10/+60° C
Internal reference:	10 MHz +/- 10 ppm
External reference:	1 V_{rms} +/- 10 dB; 1 ... 10 x 1 MHz
Spurious emissions:	$\geq$ 80 dB
Fault indication:	internal LED, external via relay contact
Auto-changeover:	operation with two synthesizer boards in parallel
	in master-slave configuration
Dimensions:	Euro-Card 100 x 160 mm

The synthesizer board (see Fig. 7.6 - 1 below and drawings 51-1584-170-00 WSP sheets 1 and 2) serves as the RF source to drive the transmitter. The synthesizer possesses two oscillators (osc. 2 of 5.76 MHz and osc. 3 of 6.8 to 13.7 MHz) and their associated PLL circuits 1 and 2. In addition, a temperature stabilized quartz oscillator (osc. 1) of 10.000 MHz is provided, which automatically switches off when an external reference frequency is applied to the synthesizer. The level of the external reference frequency shall be 1 V_{rms} +/- 10 dB sine-wave or 1 to 5 V_{pp} square-wave.

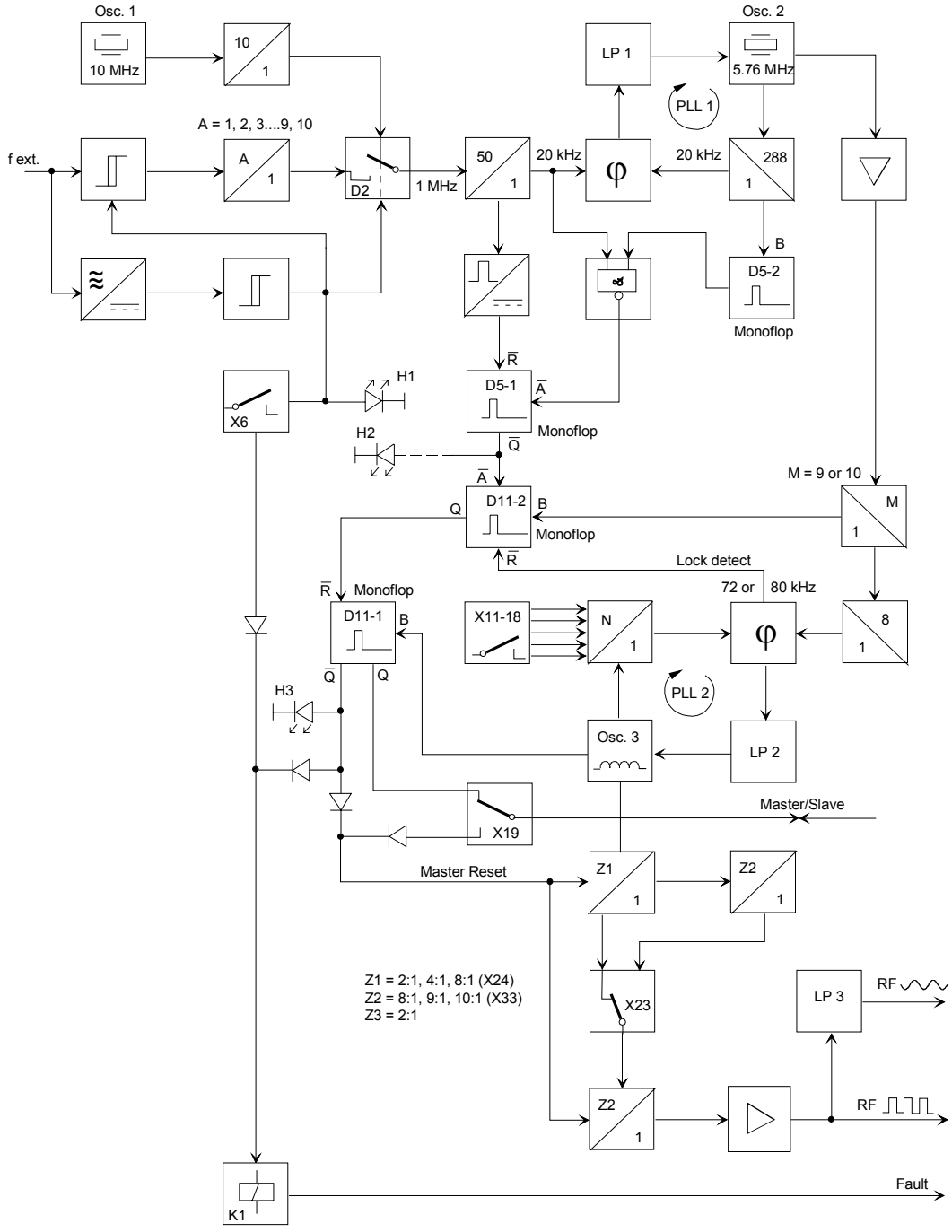

Fig. 7.6 - 1: Basic Block Schematic of the Synthesizer Board

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The RF input signal is applied to comparator D1 which drives the 16:1 divider D4-1 and to a doubling circuit comprising V1 and V2. If the RF signal has sufficient amplitude, the output voltage of D4-1 is switched through to gate D2-1 and the signal path for the internal 10 MHz oscillator is blocked. If the amplitude of the RF signal is too low, then comparator N1 blocks comparator D1 via diode V15 and blocks the signal path behind D4-1. As a consequence, the signal of quartz oscillator 1 at the output of the 10:1 divider D4-2 is applied to gate D2-1.

For operation of the synthesizer board a 1 MHz signal must be applied to MP1 (f ext.) or MP2 (f int.). Therefore the division factor of D4-1 must be set dependent on the frequency of the external RF. The four outputs of the divider can be connected to the master-reset via diodes and jumpers at X2 to X5. The reset occurs when a high signal is present at the reset input of D4-1. The divider can be set for input frequencies of 1 to 15 x 1 MHz. Table 7.6 - 1 below lists the jumper settings for X 2 to X5. For a 10:1 division, pins 2 and 3 of X3 and X5 must be jumpered. The table shows that at the tenth pulse Q1 and Q3 go high and thus a high is present at the reset input of D4-1.

Table 7.6 - 1: Division Factor Settings for D4-1

Division Factor	Q0	Q1	Q2	Q3	X2	X3	X4	X5
1	H	L	L	L	2-3	1-2	1-2	1-2
2	L	H	L	L	1-2	2-3	1-2	1-2
3	H	H	L	L	2-3	2-3	1-2	1-2
4	L	L	H	L	1-2	1-2	2-3	1-2
5	H	L	H	L	2-3	1-2	2-3	1-2
6	L	H	H	L	1-2	2-3	2-3	1-2
7	H	H	H	L	2-3	2-3	2-3	1-2
8	L	L	L	H	1-2	1-2	1-2	2-3
9	H	L	L	H	2-3	1-2	1-2	2-3
10	L	H	L	H	1-2	2-3	1-2	2-3

If the external RF is not present or fails then comparator N1 switches through the internal 10 MHz and LED H1 lights up to indicate that the external RF is missing. Should it be desired to pass an indication via relay K1 to the outside to signal that the external RF is missing then pins 1 and 2 of X6 must be jumpered.

The 1 MHz signal switched by gate D2-1 is applied to 5:1 divider D6-1 and finally to 10:1 divider D6-2. The output signal at D6-2 Q0 has a frequency of 20 kHz and a duty factor of exactly 1:1. Gate D8-1 and the 5.76 MHz crystal work together as a quartz oscillator. The oscillator frequency is applied to 16:1 divider D7-1 and finally to 144:1 divider D7-2.

The division factor is determined by diodes V10 and V11. Figure 7.6 - 2 shows the outputs of D7-1/2 and their weighting when the outputs are high. When outputs Q0 and Q3 are high, 144 pulses are counted and a reset is initiated via diodes V10 and V11. The output signal at D7-2 Q3 is passed to 2:1 divider D6-1. The signal present at the output D6-1 Q0 has a duty factor of exactly 1:1 and a frequency of 20 kHz (5.76 MHz /144 x 2).

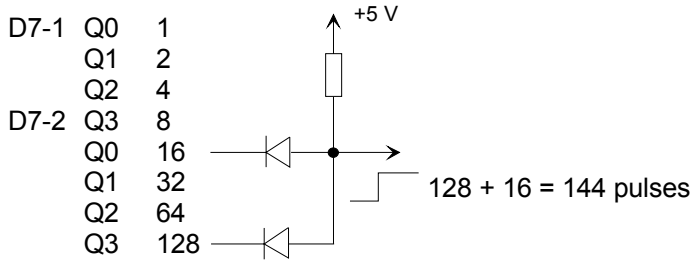

Fig. 7.6 - 2: Reset at Divider D7

Phase Locked-Loop Circuit 1 (PLL1)

Gate D3-4 functions as a discriminator. It compares the two 20 kHz voltages $f_{ref.}$ at MP4 and $f_{osc.}$ at MP3. The output voltage of D3-4 - with a duty factor of 0 to 0.5 - is filtered by the low-pass R35/C18 (LP1 in Fig. 7.6 - 1). The output voltage of D3-4 (0 to + 2.5 V) is passed through amplifier N2 to provide the closed loop control for the 5.76 MHz oscillator.

The synchronization of the 5.67 MHz oscillator with the internal 10 MHz oscillator or with the external reference is monitored with monoflops D5-1 and D5-2. D5-2 is driven with the voltage $f_{osc.}$ from MP3 and generates a needle pulse when triggered by the incoming positive edge. This needle pulse is compared in gate D3-2 with the voltage $f_{ref.}$ from MP4.

Gate D3-2 sends a pulse to monoflop D5-1 if the needle pulse coincides with the H-level of $f_{ref.}$ The pulse sequence is shorter than the reset time of D5-1 and as a result a continuous low signal is present at the inverting output of D5-1.

If the reference frequency is missing or the 20 kHz signals (MP3/MP4) are out of phase then D5-1 is no longer triggered and the inverting output of D5-1 goes high. LED H2 lights up and the RF output of the synthesizer board is blocked via D11. A failure of the 5.76 MHz oscillator is recognized with certainty by the second PLL circuit.

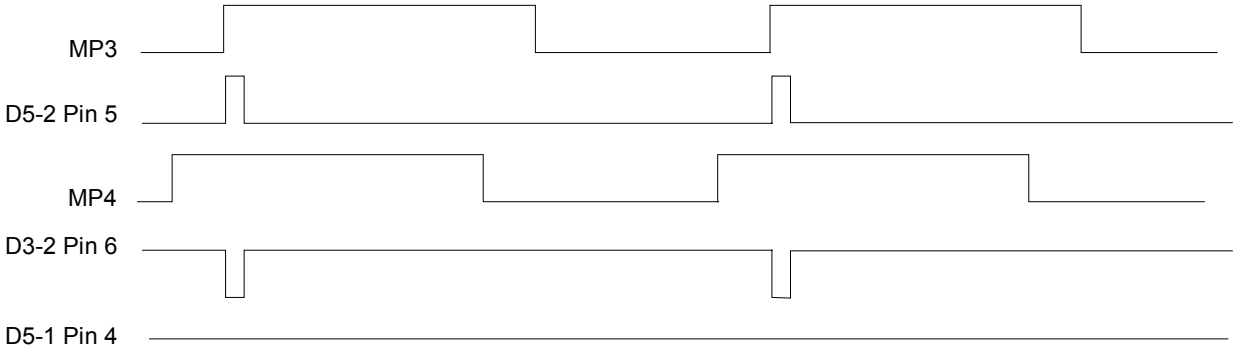

Fig. 7.6 - 3: Pulse-Timing Diagrams of PLL1

The synthesizer board must work with a channel pattern of 9 kHz or 10 kHz. The variable oscillator (osc. 3 in Fig. 7.6 - 1) oscillates with a frequency of approx. 6.8 to 13.7 MHz. The desired operating frequency is achieved by division. An 8:1 division provides a frequency of approx. 850 to 1712 kHz while a 16:1 division results in a frequency of 425 to 856 kHz. Since the division factor is equal to/greater than 8:1, the oscillator can work with a channel pattern of 8 x 9 = 72 kHz or 8 x 10 = 80 kHz. For the discriminator, one must generate 72 kHz or 80 kHz from the 5.76 MHz oscillator frequency. This is achieved by an 80:1 or 72:1 division.

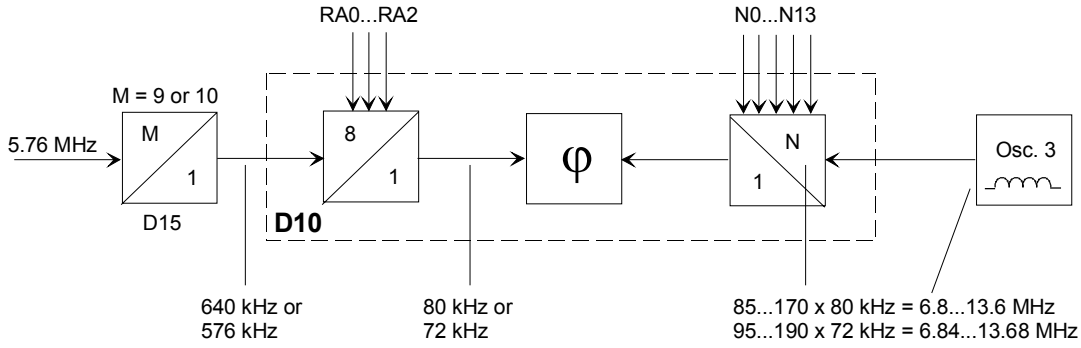

Fig. 7.6 - 4: Frequencies with 9 kHz- and 10 kHz Channel Patterns

Phase Locked-Loop Circuit 2 (PLL2)

Since the PLL device D10 already incorporates an 8:1 divider for the reference frequency, one only requires a pre-divider with a division factor of 9:1 or 10:1. This is achieved with the 16:1 divider D15. The reset occurs with the diodes V21 and V22 at 8 + 1 (Q3 + Q0) or 8 + 2 (Q3 + Q1) dependent on the jumper setting of X20 in the same manner as described above. The setting X22/1-2 results in a division factor of 9:1 and the oscillator then works with a 80 kHz pattern.

The setting X22/2-3 results in a division factor of 10:1 and the oscillator then works with a 72 kHz pattern. Because of the different frequencies of 72 kHz or 80 kHz respectively at the discriminator where comparison takes place, the N:1 divider requires various setting ranges. At 80 kHz, N is between 85 and 170 (Fig. 7.6 - 4) and at 72 kHz between 95 and 190. The variation range of the oscillator is then in both cases approximately equal.

The discriminator in the PLL device D10 delivers the control voltages (forward phase and backward phase) to integrator N3. The integrator regulates the frequency of oscillator N7 via the active low-pass N4.

The synchronization of the oscillators is monitored by monoflops D11-1 and D11-2. When the first PLL circuit (PLL1) is functioning properly, D11-2 receives a low signal from monoflop D5-1. D11-2 is triggered by the 72 kHz or 80 kHz reference frequency. The reset time of D11-2 is longer than the cycle of the reference frequency and as a consequence the output signal of D11-2 is constant.

The reset input of D11-2 is connected to the phase sync output of the PLL device D10. During normal operation D11-2 outputs a high signal. If the 5.76 MHz reference fails, or an error occurs in the first PLL circuit or PLL device D10 has a fault condition then the output of D11-2 goes low.

Monoflop D11-1 is triggered by the output voltage of the variable oscillator N7. The output of monoflop D11-2 is connected to the reset input D11-1. The reset time of D11-1 is larger than the cycle of the trigger voltage. Therefore, under normal operating conditions, the output voltage of D11-1 is constant. Pin 13 and 4 of D11-1 are at high and low respectively.

If the variable oscillator fails or if D11-2 reacts to one of the previously mentioned faults then the outputs of D11-1 change their logic status. As a result, LED H3 lights up, relay K1 picks up and the frequency divider D13 is blocked by a continuous reset.

The frequency counters D13 and D14 are connected to the buffer amplifiers V43/V36 of the variable oscillator. A division factor of 4 to 160 can be achieved by corresponding jumper settings. The principle is shown in Fig. 7.6 – 5 below.

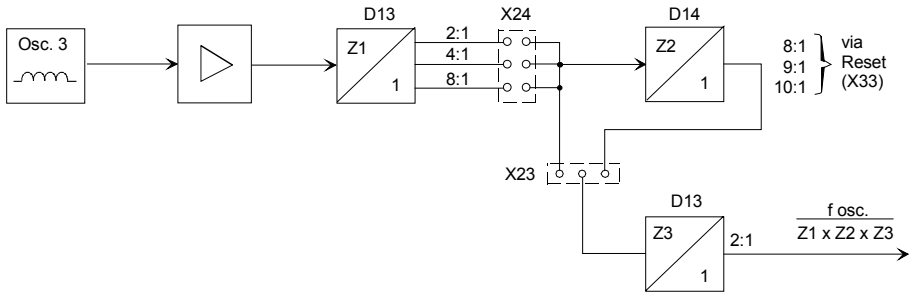

Fig. 7.6 - 5: Division of the Variable Oscillator Frequency

For MW TRAM transmitters the divider outputs 4:1 or 8:1 of D13 are used. D14 is bypassed. This gives the following output frequencies.

85...170 x 80 kHz/4 x 2 = 850...1700 kHz in 10 kHz steps
85...170 x 80 kHz/8 x 2 = 425...850 kHz in 5 kHz steps
95...190 x 72 kHz/4 x 2 = 855...1710 kHz in 9 kHz steps
95...190 x 72 kHz/8 x 2 = 427.5...855 kHz in 4.5 kHz steps

For LW TRAM transmitters the following division factors and frequencies can be set.

85...170 x 80 kHz/2 x 10 x 2 = 170...340 kHz in 2 kHz steps
85...170 x 80 kHz/4 x 10 x 2 = 85...170 kHz in 1 kHz steps
85...170 x 80 kHz/8 x 10 x 2 = 42.5...85 kHz in 500 Hz steps
95...190 x 72 kHz/2 x 9 x 2 = 190...380 kHz in 2 kHz steps
95...190 x 72 kHz/4 x 9 x 2 = 95...190 kHz in 1 kHz steps
95...190 x 72 kHz/8 x 9 x 2 = 47.5...95 kHz in 500 Hz steps
95...190 x 72 kHz/2 x 8 x 2 = 213.75...427.5 kHz in 9 kHz/4 steps
95...190 x 72 kHz/4 x 8 x 2 = 106.875...213.75 kHz in 9 kHz/8 steps
95...190 x 72 kHz/8 x 8 x 2 = 53.4375...106.875 kHz in 9 kHz/16 steps

By employing other combinations further frequencies can be set which, however, are of no importance for transmitter operation. Six inverters in parallel D12-1 to D12-6 are connected to the output of the 2:1 divider of D13. The inverters function as output amplifiers and deliver through X25/2-3 and X26 sufficient voltage to drive the RF predriver (51-1585-121-00). The output voltage of inverter D12 is a square wave and is ideal to drive the RF predriver. It is, however, not suitable to drive a phase splitting stage. The phase splitting stage is used when two transmitters in parallel operation are driven from one synthesizer. The phase splitting stage contains two mutually variable RC elements which allow the adjustment of the phase relationship of the transmitters. A proper functioning of the phase splitting stage requires that the

applied voltage is close to a sine wave. For this reason the synthesizer board incorporates a low-pass filter (switchable with jumpers) with six ranges for LW and MW (see Table 7.6 - 2 below).

Table 7.6 - 2: Frequency Ranges of the Low-Pass

Range	Frequency (kHz)	$f_{max.}/f_{min.}$
1	153...207	1.35
2	207...279	1.35
3	1287...1728	1.34
4	954...1287	1.35
5	711...954	1.34
6	522...711	1.36

With the jumper setting X25/3-4, the low-pass is connected to inverter D12. Due to the duty factor of 1:1 even harmonics are practically non-existent in the output voltage of D12. The low-pass is conceived for the attenuation of 3f. An impedance converter formed by emitter followers V39 and V42 at the output of the low-pass delivers a voltage of approx. 1 V_{rms} across 50 Ω to the downstream load.

Some transmitter operators require the use of two RF generators with auto switchover. The synthesizer board is prepared for parallel operation.

In parallel operation, the RF inputs and -outputs are connected in parallel and the terminals X34/2 and X31/a4 of both synthesizer boards connected to each other. The jumper setting of X19 on the boards then determines which board is to act as master (X19/2-3) and which as slave (X19/1-2).

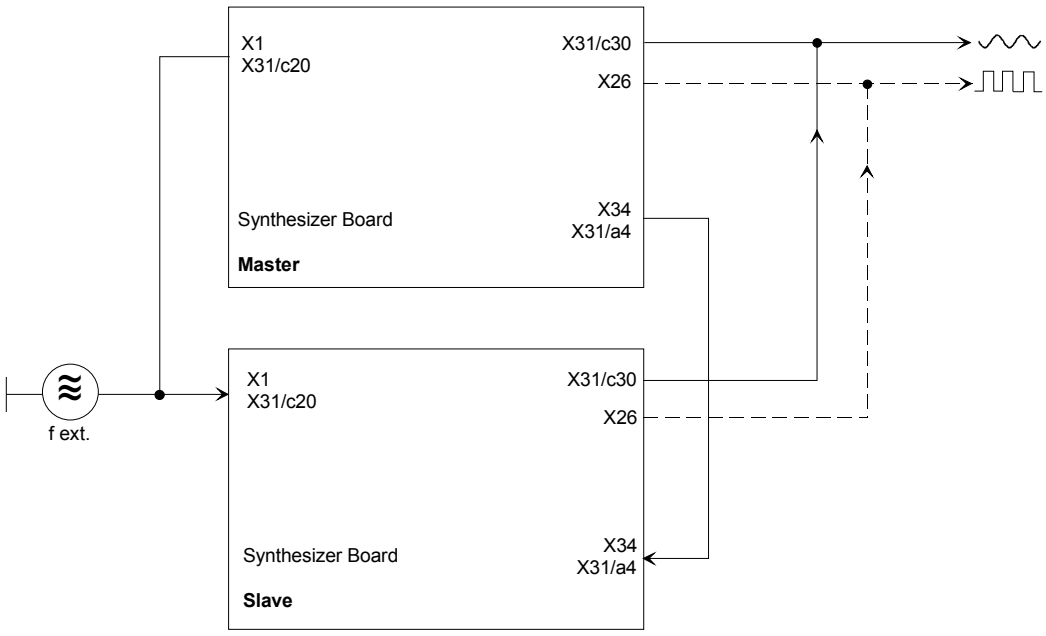

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Fig. 7.6 - 6: Parallel Connection of the Synthesizer Boards

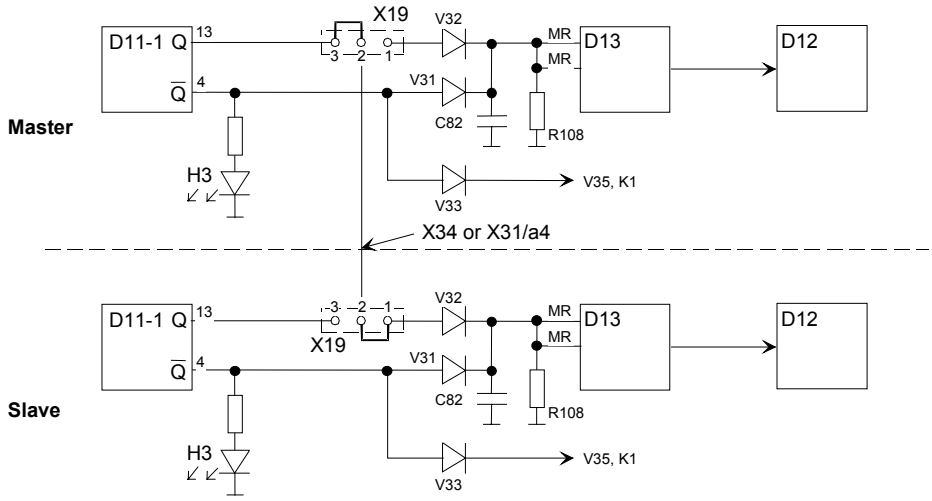

Fig. 7.6 - 7: Auto Changeover Circuit

As described above, the oscillators are monitored by a series circuit of four monoflops. Normally D11-1 as the last monoflop in the series circuit is continuously post-triggered so that pin 13 is high and pin 4 is low. Fig. 7.6 - 7 shows the principle of auto changeover. If both synthesizer boards are operating properly then D11-1 pin 4 is low and D11-1 pin 13 is high in both boards. The high signal from D11-1 pin 13 of the master board is passed via jumper X19/2-3 and routed to the slave board where it is applied via X19/1-2 and diode V32 to the master reset input of D13. As a consequence D13 blocks and the slave board cannot deliver RF. Under this condition, if a fault occurs in the slave board then LED H3 lights up and relay K1 issues a fault indication. If a fault occurs in the master board, D11-1 changes its logic state, pin 4 goes high and blocks, via diode V31, frequency divider D13, LED H3 lights up, relay K1 issues a fault indication and the master board does not deliver RF. Pin 13 of D11-1 is now low. This signal is passed to the slave board which releases the RF.

Due to the parallel connection of synthesizer boards, the drive voltage for the downstream stage is smaller. With a source impedance of 50 Ω and a 50 Ω load, the drive voltage changes from 1 V_{rms} to 0.67 V_{rms}. This, however, is sufficient to drive a phase splitting stage or an RF predriver.

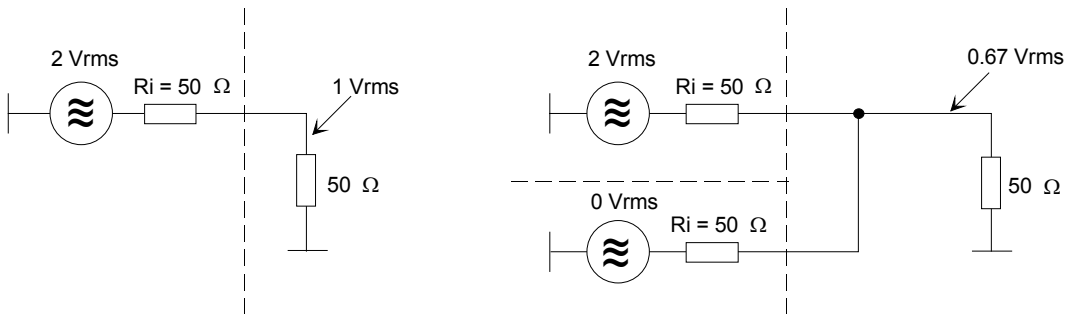

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Fig. 7.6 - 8: Output Voltage of a Synthesizer Board (Single and Parallel Connection)

A reduction in voltage also occurs at the input side when two parallel connected synthesizer boards (each with of 50 Ω internal impedance) are driven by an external reference frequency (see Fig. 7.6 - 9). If the RF level to drive a single synthesizer is relatively low, then it may not be sufficient to drive two boards.

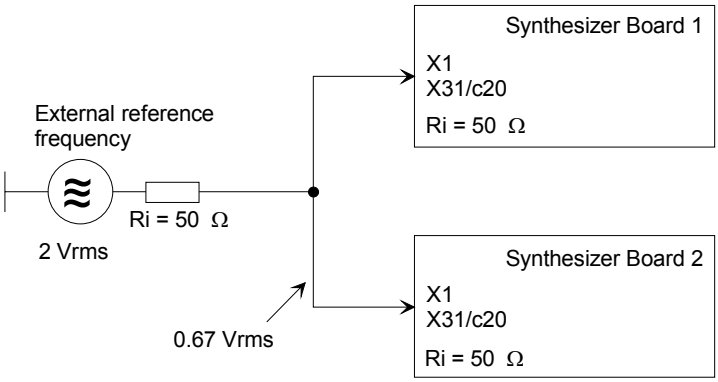

Fig. 7.6 - 9: External Reference Frequency Drive of Two Synthesizer Boards

Preparations have been made for the case that the TRAM transmitter shall be driven by an external synthesizer (Fig. 7.6 - 10). An external synthesizer can be connected to X31/c24 or X27 of the board. The RF signal of the external synthesizer is routed to the RF output X31/c30 or X26 by re-jumpering X32 or X25.

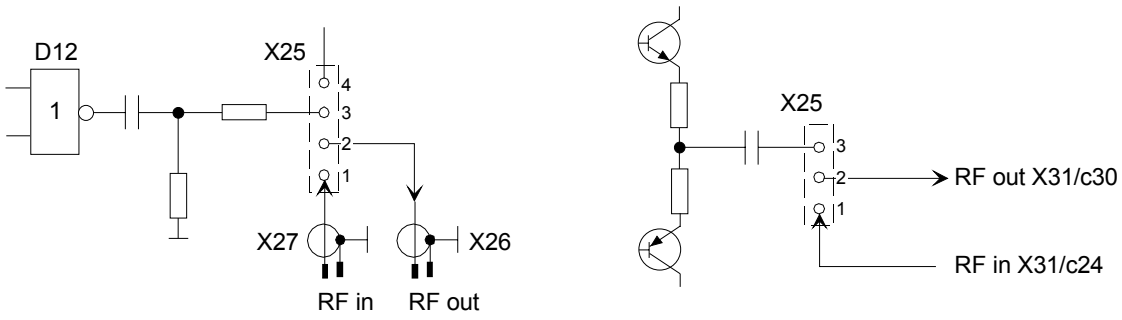

Fig. 7.6 – 10: Connections for an External Synthesizer

Power for the synthesizer board is delivered by auxiliary voltage supply 1 (51-1584-260-00) of the TRAM transmitter. The board receives three unstabilized voltages +18 V, +9 V and -18 V. Voltage regulators N5 and N6 on the board generate +5 V and - 5V supplies.

The unstabilized DC voltages and the RF voltage from X25 pin 2 are also fed to connector X28. The phase comparator 51-1584-240-00 can be connected here.

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7.7 Processing the RF Signal

The RF predriver works on the same principle as the power modules in the RF final stage. Here, however, no special requirements exists for linearity and frequency response.

The amplitude of the RF signal generated by the synthesizer is not sufficient to drive the RF amplifier (H-bridge) so that the signal must be amplified (the amplitude should lie in the range 1 V ± 10 dB).

A preliminary amplification takes place with comparator D9 which converts the RF input signal into two square-wave shaped output signals in phase opposition, each having a constant amplitude of approx. 5 V. Fluctuations in the RF input amplitude are thus removed.

The square-wave output signals, however, are not suitable to drive the downstream push-pull amplifiers (half-bridges) comprising transistors V21 and V22: when switching, an overlap of the switch-on times of the transistors would result. As a consequence, high short circuit current transients would be formed which could excite high frequency self-oscillations. In order to prevent overlapping, a dead time Δ t must be incorporated between the switch-off time of one transistor and the switch-on time of the other (Fig. 7.7 - 1 C).

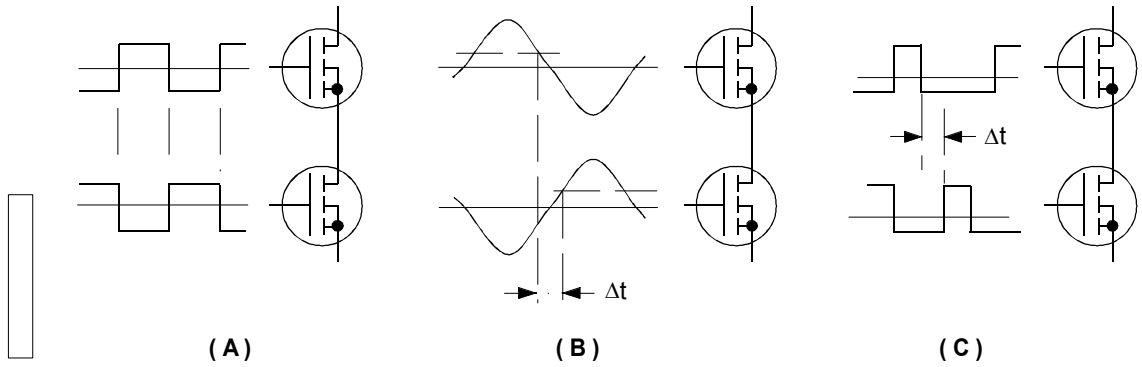

Fig. 7.7 - 1: Drive Signals for the Push-Pull Amplifiers

This could be achieved with a sinusoidal drive: the transistors would first conduct with a threshold voltage of approx. 2 to 4 V so that the dead time would be given by the form of the drive voltage curve (Fig. 7.7 - 1 B).
Since, however, the output signals of the comparator have a square-wave form and the amplifier is required to operate without tuning circuits, the pulse width of the square-waves must be altered (Fig. 7.7 - 1 C): the output signals of comparator D9 and gates D5/1 and D5/2 respectively, the latter serve only to

block the RF signal path, are passed to gates D5/3 and D5/4, once by a direct path and once through an RC combination. The values of the RC components determine the change in pulse width at the output of gates D5/3 and D5/4 (Fig. 7.7 - 2). The pulse width change at D5/3 and D5/4 can be influenced by potentiometer R54.

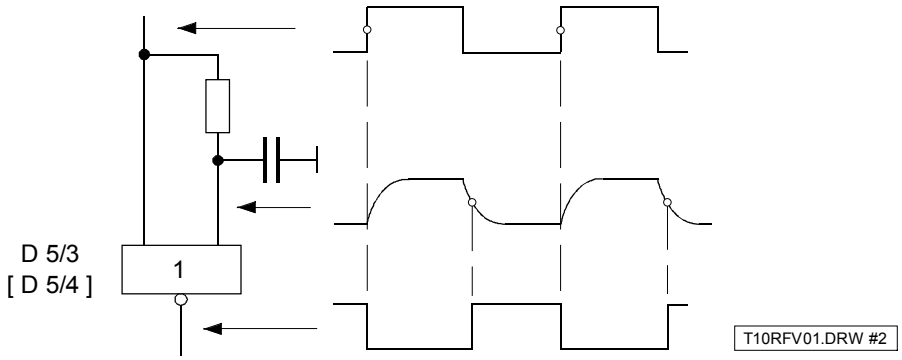

Fig. 7.7 - 2: Pulse Shape at the Output of Gates D5/3 and D5/4

The MOSFET drivers D7 and D8 are driven with the output voltages of gates D5/3 and D5/4. Due to their high operating frequency, up to 1.6 MHz, the drivers may only work with an operating voltage of max. 5 V otherwise the internal switching losses would be too high. The drivers D7 and D8 provide a common drive, via transformer T1 for the half-bridges comprising V21 and V22 (Fig. 7.7 - 3). V21 and V22 deliver the drive power for the RF power amplifier (H-bridge) comprising MOSFETs V23 to V26. The resistor circuit R57 to R64 together with the input capacitance of the H-bridge ensure that switching time overlap also does not occur in the H-bridge.

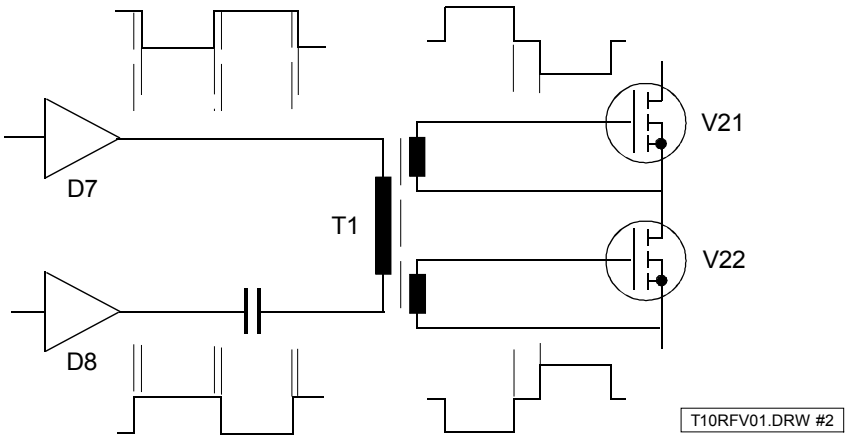

Fig. 7.7 - 3: Drive Circuit for the RF Amplifier

7.8 Combiner / Output Filter

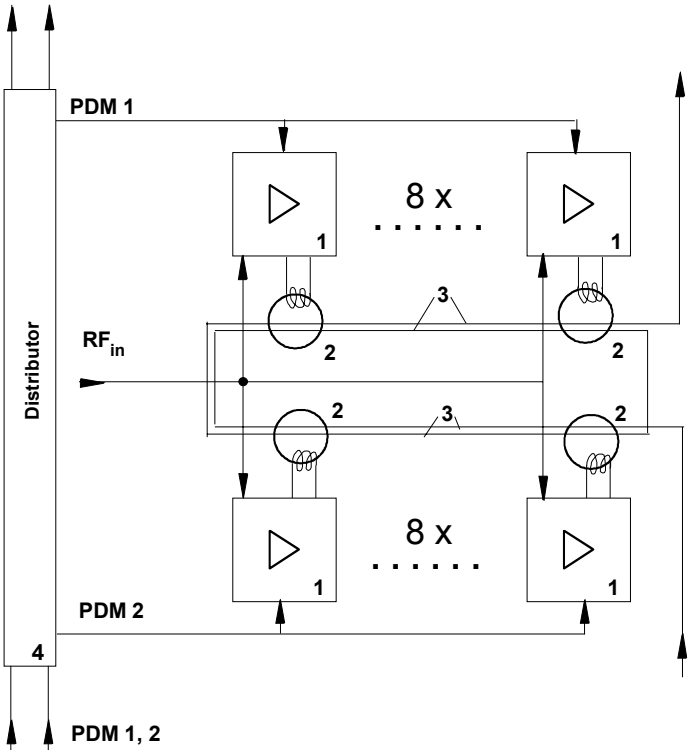

Fig. 7.8 - 1: Combiner Circuit

[1] Amplifier modules, [2] Combiner coils, [3] Aluminium bars, [4] Distributor

The outputs of the 96 amplifier modules [1] are summed in a series transformer circuit. Each amplifier module output is connected to a ring-core transformer (combiner coil) [2]. Aluminium bars [3] through the cores form the secondary windings of the transformer.

The secondary conductor is passed two times through the cores of blocks of 16 power modules. The blocks are connected in series to provided the total output power of the transmitter.

The output signal is applied to the output filter [8] in Fig. 7.8 - 2. The filter is tuned so that only the high frequency fundamental is passed and the harmonics of the switching frequency are suppressed. At the transmitter output a capacitive voltage divider [9] is used to couple out a test signal to allow measurements of the modulation factor and monitor signal quality. This is accomplished by a demodulator located in the AF stage [11] of the transmitter and test output X3 in the control panel which delivers a test voltage proportional to the output voltage.

The feed line monitor [10], also located at the transmitter output, delivers dc voltages proportional to the forward- and reflected powers. These voltages are used to measure the matching of the transmitter load and the power output of the transmitter. The respective evaluation takes place in the output monitor [13] located in the control cabinet.

Under high mismatch conditions, transmitter output power is reduced by changing the duty factor of the PDM pulses in the AF stage [11] or the transmitter is shut down. The cross-point meter in the control panel [12] displays the output power and the mismatch.

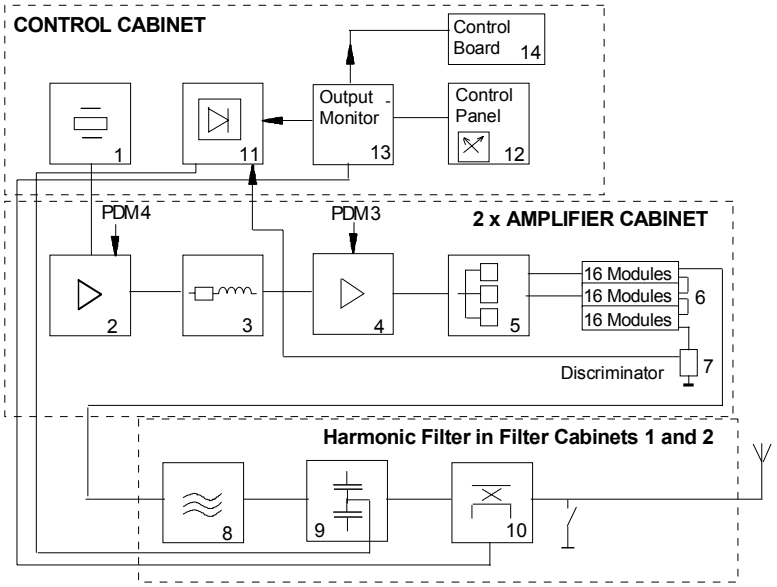

Fig. 7.8 - 2: Simplified Block Schematic of Signal Paths in the Transmitter

A discriminator [7] is located at the low-end of the combiner. It delivers a voltage proportional to the phase of the load impedance. The signal is evaluated in the output monitor and displayed by the tuning meter in the control panel.

A grounding switch is located directly at the transmitter output. It is engaged by rotating its lever after the switch has been released by the key interlock system.

1	Synthesizer Board	8	Output Filter
2	RF Predriver	9	Voltage Divider
3	Series Damping Circuit 1	10	Feed Line Monitor
4	Driver	11	AF Stage with Diode Detector
5	Series Damping Circuit 2	12	Control Panel
6	48 Amplifier Modules per Amplifier Cabinet	13	Output Monitor
7	Discriminator	14	Control Board

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Transmitter tuning is optimized with the aid of the tuning meter and the variable coils of the harmonic filter. An RF current transformer is mounted on the discriminator which delivers a voltage proportional to the high frequency current flowing through the combiner. When the threshold value is exceeded the control board issues the indication I-RF > and shuts down the transmitter.

RF drive of the amplifier modules takes place through the synthesizer board via the predriver, its series damping circuit, the downstream drivers in amplifier cabinets 1 and 2 (of the same design as the amplifier modules) and a further series damping circuit whose three outputs are connected via three inductances to the amplifier blocks. The inputs of the 96 amplifier modules arranged in 6 blocks of 16 modules are connected in parallel and are driven in common.

8 CONTROL FUNCTIONS

8.1 Local- , Remote Control and Blocking the Keyboard

Local-, remote control and blocking the keyboard are explained with reference to drawing 51-1584-121-00 WSP. In local mode, the transmitter is controlled through the keyboard via connector X90.

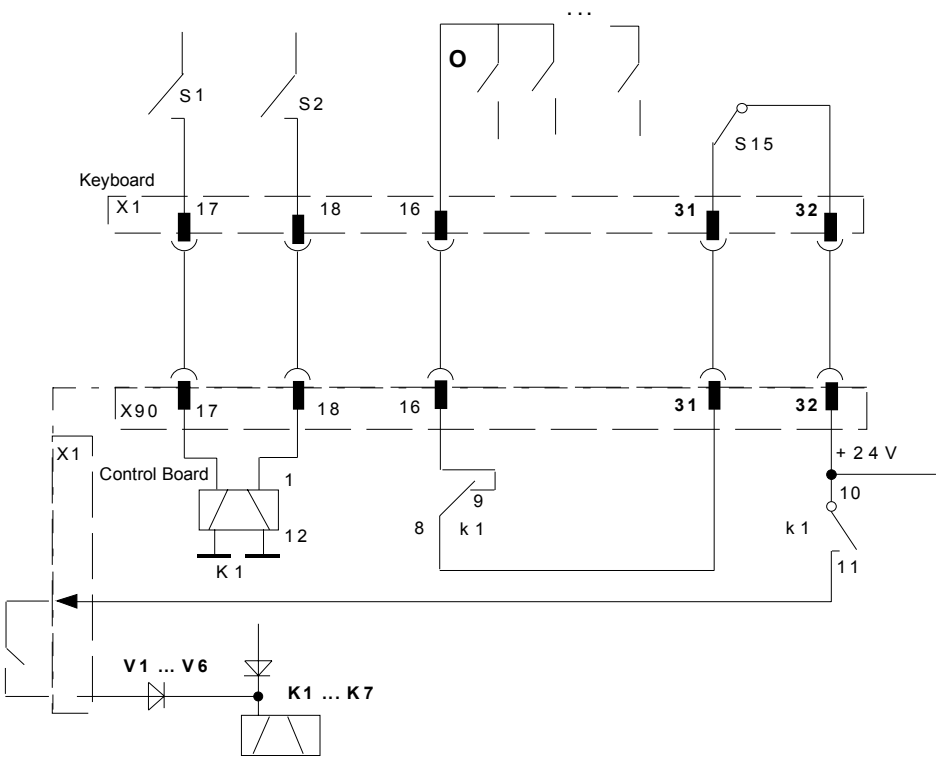

Fig. 8.1 - 1: Circuit for Local- Remote Switching and Keyboard Blocking

Local mode is activated by pressing key S1 of the keyboard. Relay K1 resets and applies the auxiliary voltage of +24 V via contacts 8, 9 to the contacts in the keyboard and disconnects the +24 V to the remote control interface via contacts 10, 11.
Remote mode is activated by pressing key S2 of the keyboard. Windings 1, 12 of K1 are energized and contacts 8, 9 open which disconnect the +24 V supply to the keys in the keyboard except for the "Clear " key S14. Contacts 10, 11 of K1 close and apply +24 V to the remote control interface via X1/16. As a consequence, closed contacts of remote control equipment can activate relays K1 to K7 via X1 and diodes V1 to V6. Status indications (via connector X3) for remote control equipment are passed by contacts of relays K1..K8, K10..K13, K15 and K16.

The keyboard can be blocked (locked) by slide switch S15 which then disconnects the +24 V supply to the keys. This is signaled by LED H14.

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8.2 Transmitter On/Off Switching

Local transmitter switch on is made by pressing key "I P1" for max. power or key "I P2" for reduced power after the main switch in the control cabinet has been manually engaged (400 V mains switched through). The keys apply 24 V via decoupling diodes in the keyboard and decoupling diodes V19 or V18 in the control board to a winding of bistable relay K2 in the control board.

In remote mode, the 24 V needed to switch K2 is applied via diodes V10, V19 or V9, V18.

After switch-on, contact 8, 9 of K2 opens and this condition is interrogated by gate D21/3. When "I P1" or "I P2" is pressed a low is present at the input of the gate and the output is high. The high signal is switched through by AND-gate D15/1 as long as no summary fault signal is present which would block D15/1 with a low at the second input.

Relay K9 is activated through transistor V107 and the series connection of contacts K16 (4/5) and K10 (2/3) and energizes via the switch-on delay boards A7200/A7500, auxiliary contactor K7100 and K7400 in the control cabinet. These contactors switch through the supply voltage for the transmitter, via resistors R8110, R8120, R8130/R8150, R8160, R8170 in the control cabinet, to transformers T5400 in the amplifier cabinets. After a time delay of approx. 2 s the main contactors K7000 and K7300 are energized and switch the supply voltage directly to the transformers. This "soft" start limits the switch-on current brought about by the charging of the filter capacitors and prevents the rush of an overcurrent and the burn out of the fuses in the RF predriver, drivers and amplifier modules when the transmitter is switched on. The switch-on process as described above is prevented when

- the door contact of one of the amplifier cabintes is closed (i.e., a door is opened),
- the mains monitor opens contact 4, 5 of relay K16,
- a summary fault signal stored by relay K10 causes its contact 2, 3 to open
- one input of gate D15/1 is switched to low by a fault evaluation circuit.

This means that when a summary fault occurs the transmitter is switched off and cannot be switched on again until relay K10 is reset.

The mains monitor does not pass a summary fault signal but switches the transmitter off through contact 4, 5 of relay K16 when it detects a fault in the mains supply. When mains is again restored, contact 4, 5 closes and the transmitter is "soft" started by means of auxiliary contactors K7100 and K7400.

Bistable relay K10 can only be reset by pressing the "Clear" key S14  . When relay K2 has picked up (On command) the transmitter is immediately switched on again without further intervention.

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The transmitter is switched off by pressing key S3 "**O**". This resets relay K2 thus breaking the switch-on sequence. In remote mode, K2 is reset via decoupling diode V11 in the control board.

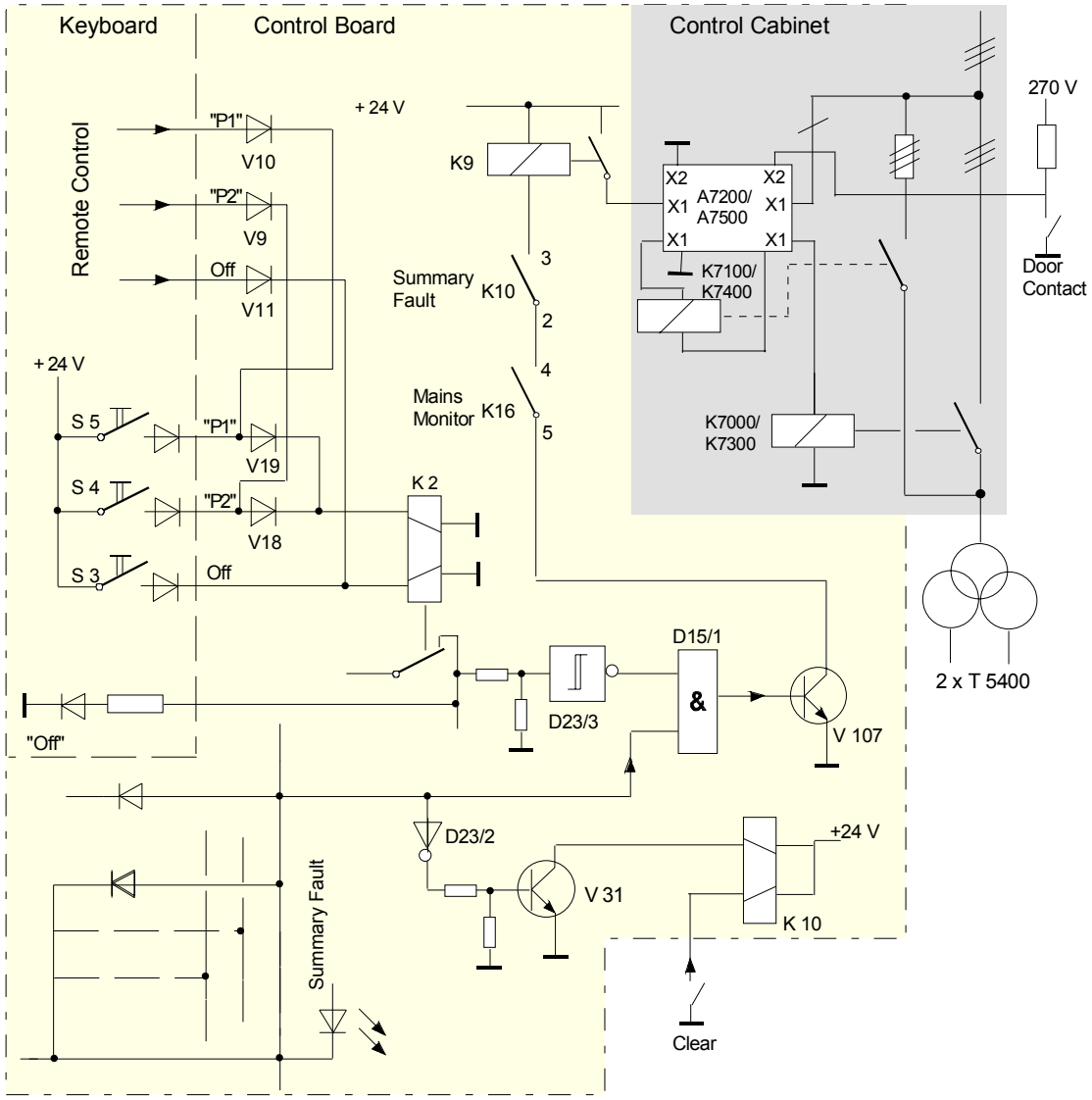

Fig. 8.2 - 1: Transmitter On/Off Switching

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8.3 PDM Enable/Inhibit

The PDM pulses of the amplifier modules can be enabled or inhibited by pressing keys S7 "I PDM“ and S6 "O PDM“ respectively.

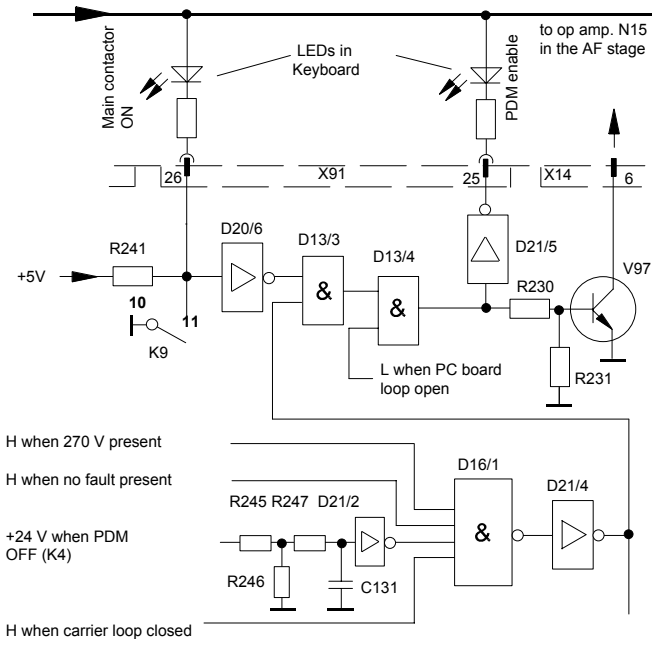

Fig. 8.3 - 1: Schematic Circuit of PDM Inhibit on the Control Board

The PDM enable/inhibit keys act on bistable relay K4. With PDM inhibit, contact 8, 9 of K4 passes +24 V via voltage divider R245, R246 to the input of inverter D21/2, its output goes low which blocks gate D16/1 independent of the signals at the other inputs. After double inversion (output; gates D16/1 and D21/4) the low signal is passed through gates D13/3 and D13/4 to transistor V97. The signal at the collector is applied through terminal X14/6 to initiate PDM inhibit in the AF stage.

PDM pulses can only be enabled through relay K4 when a high signal is present at all inputs of gates D16/1, D13/3 and D13/4, i.e.,

- an indication is issued that the 270 V supply is available,
- no faults have been registered,
- relay K 4, which stores the PDM enable command, has picked up,
- the external carrier loop is closed,
- the PC board loop is closed and
- the switch-on command, which energizes the main contactor through relay K9, has been signaled by its contact 10, 11.

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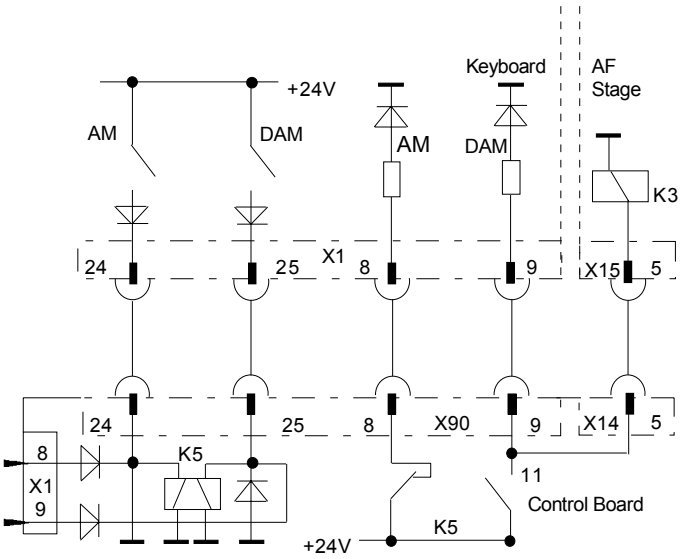
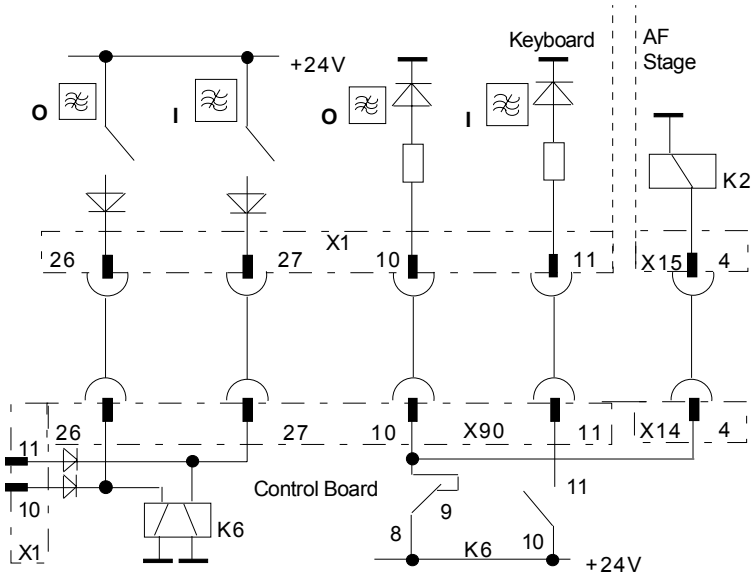
8.4 On/Off Switching of AM and DAM Modes



Carrier control for DAM operation is switched on or off in the AF stage with keys S9 (DAM) and S8 (AM) respectively or through the corresponding connections of the remote control interface (via X1). Bistable relay K5 in the control board stores the desired state which is signaled by the respective LED in the key. The +24 V supply is switched to the AF stage through terminal X14/5 when DAM is selected and carrier control in the AF stage is activated through relay K3.

Fig. 8.4 - 1: Simplified Circuit Diagram for On/Off Switching of AM and DAM Modes

8.5 On/Off Switching of the Low-Pass Filter



One of the low-pass filters in the AF stage is switched on or both are bypassed with keys S11 and S10 respectively or through the corresponding connections of the remote control interface (via X1). Bistable relay K6 in the control board stores the desired state which is signaled by the respective LED in the keyboard. The +24 V supply is switched to the AF stage through terminal X14/4 and the respective low-pass filter is switched on or bypassed by the action of relay K2.

Fig. 8.5 - 1: On/Off Switching of an AF Low-Pass Filter

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8.6 Selection of an AF Low-Pass Filter

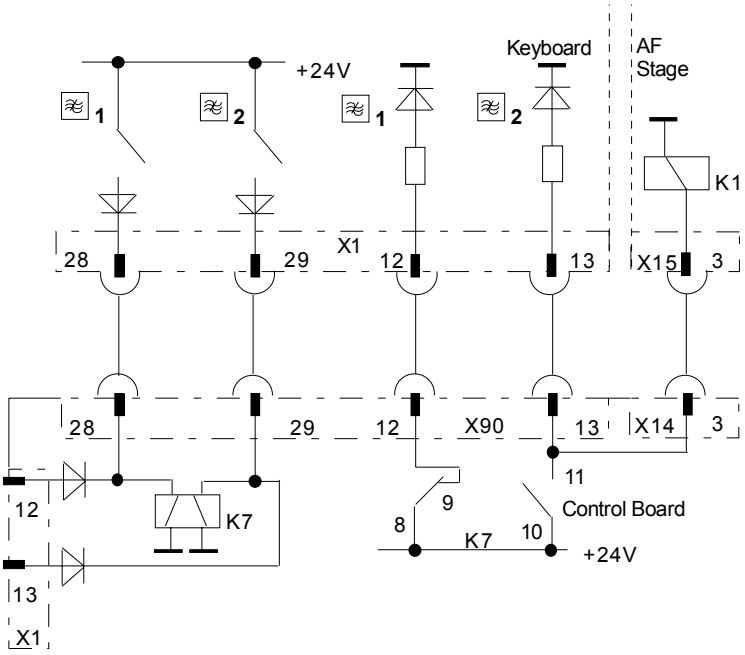

Fig. 8.6 - 1: Selection of an AF Low-Pass Filter

One of the two low-pass filters in the AF stage is selected with keys S12 and S13 or through the corresponding connections of the remote control interface (via X1). Bistable relay K7 in the control board stores the desired selection which is signaled by the respective LED in the keyboard. The +24 V supply is switched to the AF stage through terminal X14/3 and the respective low-pass filter is selected by the action of relay K1. The selected filter is only effective when S11 as described above is pressed.

9. MEASUREMENT AND MONITORING

The control board of the transmitter serves to measure and monitor operating parameters. Monitoring- and evaluation circuits incorporated in the control board issue warning- or fault indications and if necessary transmitter shutdown is initiated. Measurements are performed by amplifier circuits whose outputs are passed to monitoring circuits. Status indications are provided by LEDs in the control panel.

9.1 Monitoring Circuit

The monitoring circuit essentially comprises a comparator [1], storage device [2] and a display element [3] (see Fig. 9.1 - 1). The test voltage U_{in} is monitored by the comparator. If this voltage exceeds a reference U_{ref}, the comparator responds and its output switches to about zero potential. As a result, the output of gate [2] goes low. This state is maintained until the output of the comparator is again high and the second input of the gate is switched high either by a "Clear" pulse or a continuous high signal. The fault indication is passed via diode [4] for further processing and signaled by diode [3].

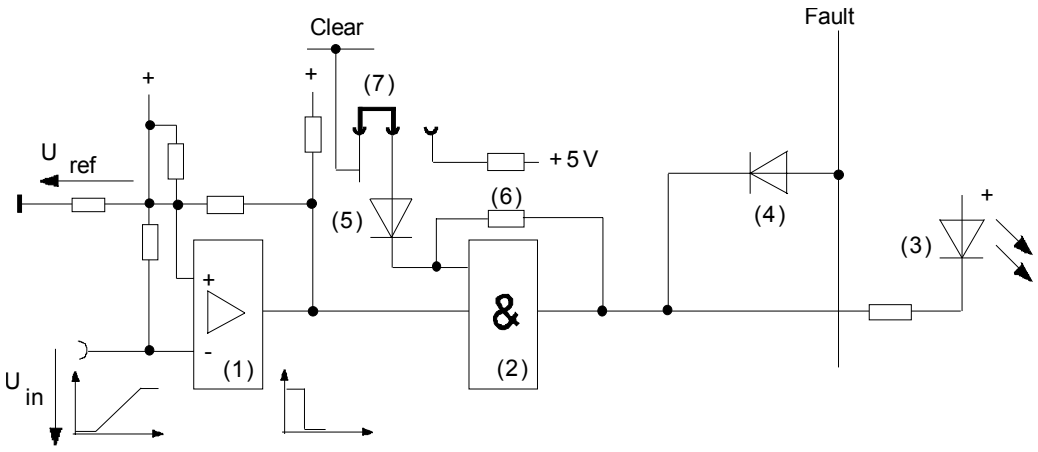

Fig. 9.1 - 1: Monitoring Circuit

If diode [5] is connected to +5 V by jumper [7] the output of gate [2] will always be in the same state as the output of the comparator and as a consequence it looses its storage effect.

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9.2 Evaluation Circuit

An evaluation circuit is incorporated in the cabinet monitoring boards and control panel. Operating parameters of the amplifier block are monitored by the respective cabinet monitor evaluation circuit and when deviations from normal operating conditions occur a fault indication is issued. These are passed through decoupling diodes [1] and via the parallel connection of both cabinet monitors as a summary fault to the control board.

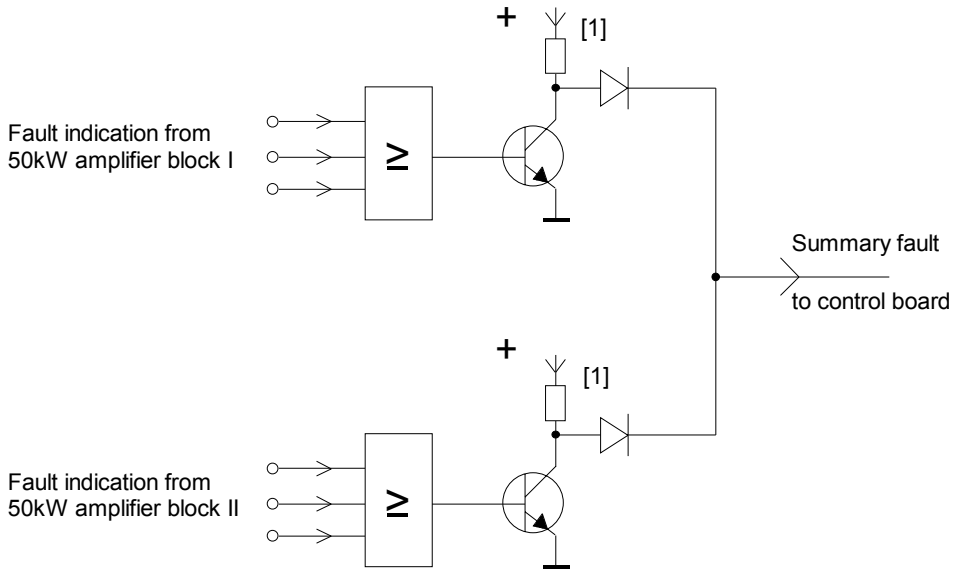

Fig. 9.2 - 1: Evaluation Circuit of the Cabinet Monitors

The evaluation circuit on the control board signals deviations from normal transmitter operation through the LEDs in the control panel and through the remote control interface. Depending on the magnitude and type of deviation, warning- and fault indications are issued and if necessary the transmitter is shut down. The logical principle of this circuit is shown in Fig. 9.2 - 2.

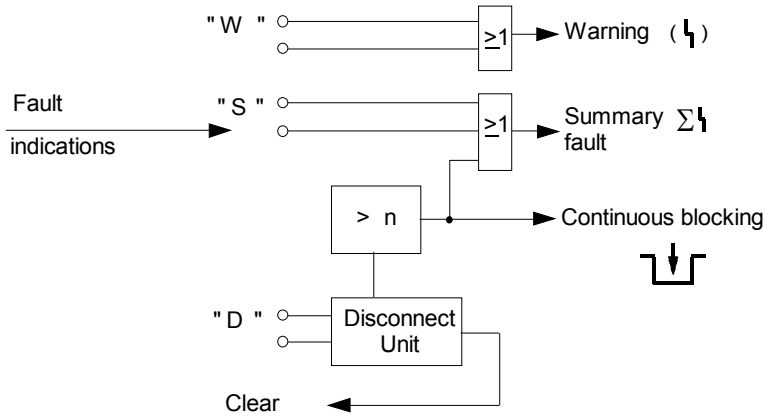

Fig. 9.2 - 2: Evaluation Circuit on the Control Board

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9.3 Warning Indications

Warning indications are issued when it is determined that the transmitter deviates from normal operation, however, transmitter components are not endangered. The transmitter does not shut down and the indication is signaled by a LED.

A warning indication results in fault evaluation circuit 1 responding (see Fig. 9.5 - 1). The output of this circuit is connected to the line "NOT WARNING". When a warning is recognized, the line goes low and transistor V93 blocks. This causes relay K13 to drop out. The contacts of the relay pass this indication to the respective LED in the control panel and also to the remote control interface.

Warning indications are designated by the letter "W" in column "!" of the fault table in Annex 2.

9.4 Mains Interruption

When a mains fault occurs, the mains monitor recognizes the failure of one or more phases and issues an indication. The fault evaluation circuit consisting of D4/2 and D11/4, corresponding to fault evaluation circuit 2 in Fig. 9.5 - 1, causes the line "NOT INTERRUPTION" to go low and as a result transistor V94 blocks and relay K16 drops out. The indication is passed to the remote control interface via contacts of K16 and signaled in the control panel - LED "Mains present" turns off. In addition the switch-on sequence is broken via contact 4, 5 of K16 which causes relay K9 to drop out and as a consequence the main contactors of the transmitter trip - PDM blocking is also initiated.

The behaviour described above occurs with faults designated by the letter "U" in column "!" of the fault table in Annex 2.

PDM Blocking

If the fault evaluation circuit for the external carrier loop consisting of D3/4 and D11/2 responds, (see fault evaluation circuit 4 in Fig. 9.5 - 1) the line NOT PDM goes low which blocks the PDM pulses in the AF stage via the action of gates D16/1, D21/4, D13/1...D13/4, transistor V97 and op amp. N15. Pulse blocking turns off the LED "PDM" in the control panel. This indication is not sent to remote control equipment or stored in a bistable relay.

PDM blocking can also be initiated by the cabinet monitors. PDM enable via distributor 2 takes place through relay K9 when the transmitter switch-on command is given and the 270 VDC is present in both amplifier cabinets (see Fig. 9.2 - 1(c)).

Due to the logical interconnection of both cabinet monitors by means of diodes, PDM enable can only occur through comparator D1/2 in the control board. This ensures that the PDM pulses can first be released only when both amplifier cabinets are supplied with 270 VDC. LED H1 of the cabinet monitor signals switch-on readiness, while LED H2 signals readiness for PDM release.

The behavior described above occurs with faults designated by the letter "P" in column "!" of the fault table in Annex 2.

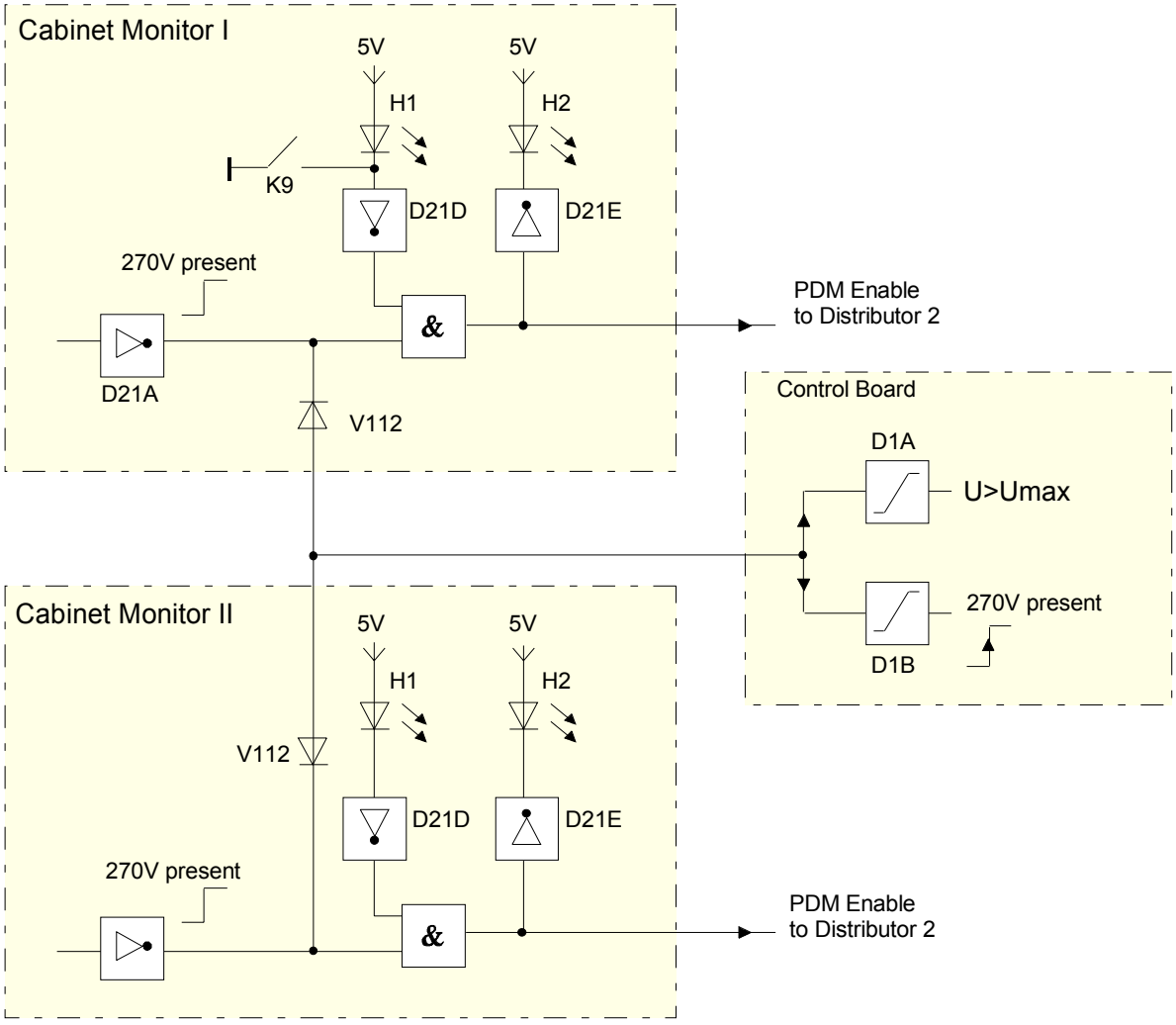

Fig. 9.4 - 1: PDM Blocking/Enable via the Cabinet Monitors

The behaviour described above occurs with faults designated by the letter "P" in column "!" of the fault table in Annex 2.

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Summary Fault Indication

Deviations from normal operation which could endanger the transmitter or its components result in a summary fault indication and simultaneous PDM blocking or transmitter shutdown.

If the summary fault evaluation circuit responds due to a major fault (see fault evaluation circuit 5 in Fig. 9.5 - 1), the line NOT SUMMARY FAULT goes low and the switch-on sequence is broken at gate D15/1 which causes the main contactor of the transmitter to drop out. The summary fault signal is passed via inverter V23/2 and transistor V31 to bistable relay K10 and stored. This condition remains until K10 is reset by the "Clear" key in the control panel.
The summary fault indication $\Sigma!$ is displayed in the control panel and passed to the remote control interface X3.

The behaviour described above occurs with faults designated by the letter "S" in column "!" of the fault table in Annex 2.

9.5 Continuous Blocking

Non-critical faults which can be rectified by a short interruption in operation (e.g., flashover in the antenna and consequently high mismatch) lead to PDM blocking and thus blocking of the RF output power. These faults act on the reconnecting unit (V69, V75, V88, V89, V90, V91 in drawing 51-1584-121-00 WSP).

When such a fault occurs, fault evaluation circuit 3 (see Fig. 9.5 - 1) responds and the line NOT FAULT goes low. As a result PDM blocking takes place in the AF stage via the action of series circuit D16/1...D13/4 functioning as an AND gate, transistor V97 and op amp. N15. Simultaneously the reconnecting unit is activated. After about 2 s the reconnecting unit outputs a "Clear" pulse which resets the fault evaluation circuit through D23/3, V104, D20/5 and D20/1. The PDM pulses are again enabled if "Reset" was accomplished.

If the fault is still present despite the reset pulse or the fault occurs repeatedly within a set time window then the reconnecting unit issues the continuous blocking signal. No further reset pulses are output. The number of reset pulses within the time window is selectable by means of a jumper.

The continuous blocking pulse of the reconnecting unit initiates a summary fault i.e., the line NOT SUMMARY FAULT goes low due to the action of inverter D23/1 and diode V112. The summary fault signal is passed via inverter V23/2 and transistor V31 to bistable relay K10 and stored.

The summary fault results in the switch-on sequence being broken at gate D15/1 which causes the main contactor of the transmitter to drop out. This condition remains until K10 is reset by the "Clear" key in the control panel. The summary fault indication is displayed in the control panel and passed to the remote control interface X3.

Continuous blocking is displayed by diode H19 ⊓↓⊓ in the control panel. The continuous blocking signal is not passed to remote control equipment or stored.

The behaviour described above occurs with faults designated by the letter "D" in column "!" of the fault table in Annex 2.

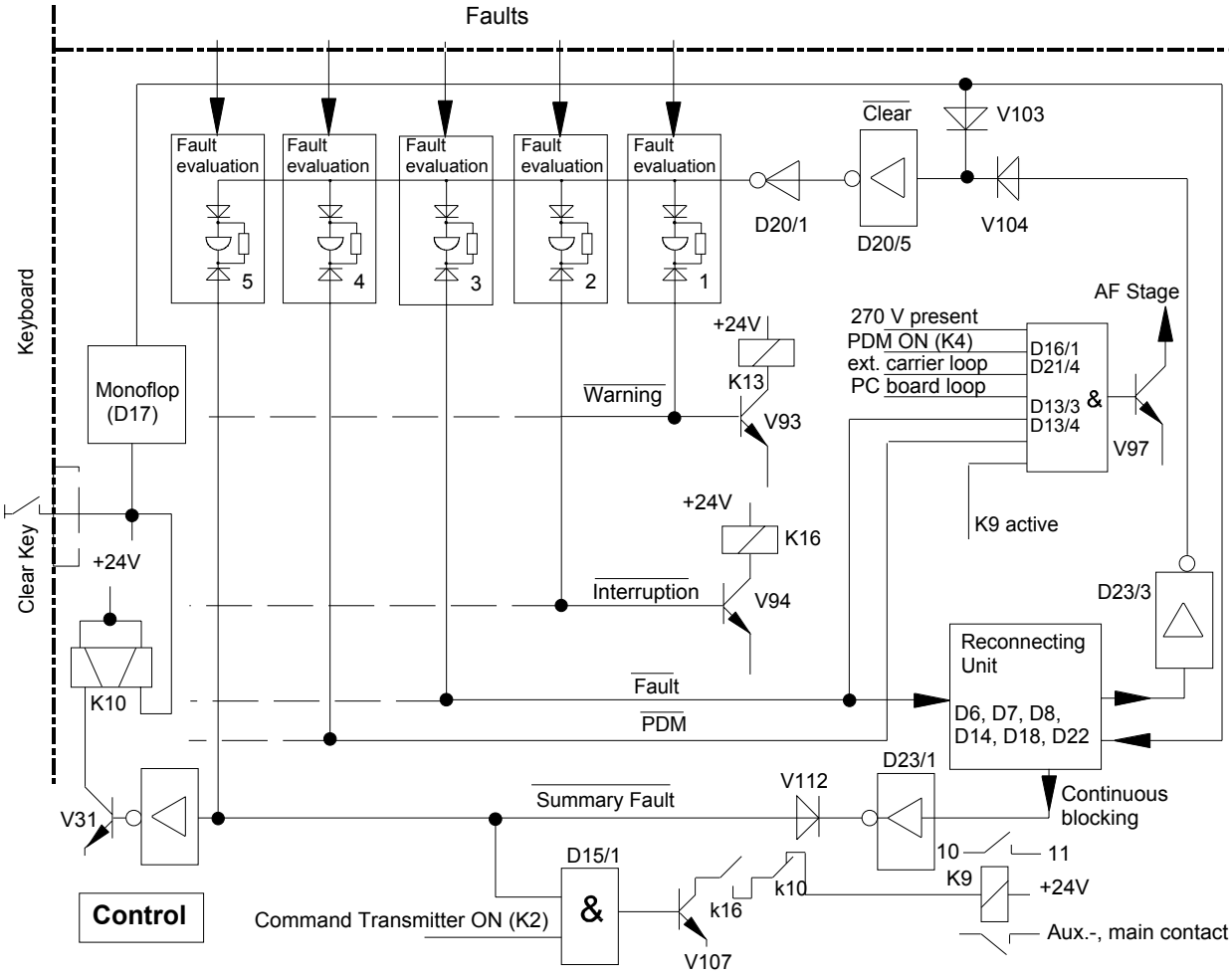

Fig. 9.5 - 1: Simplified Block Schematic of the Fault Evaluation and Control Circuits

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9.5.1 Reconnecting Unit

(See also drawing: 51-1584-121-00 WSP sheet 9)

The reconnecting unit is a circuit in the control board which switches the transmitter on again after a shut down caused by a fault (e.g. S>, I_{RF} >). The reconnecting unit sends a "Clear" pulse to the fault evaluation circuit in the control board. The number of reconnecting attempts (trials) is selectable by means of a jumper. If the trials are unsuccessful, the signal "Continuous blocking" is output and the transmitter remains in the shutdown state.

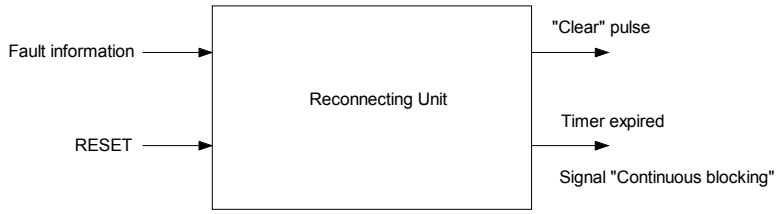

Fig. 9.5.1 - 1: Basic Principle of the Reconnecting Unit

The reconnecting unit incorporates a counter (74HC4017), two counters (74HC4060) with internal oscillators and various gates. The counters with oscillators (D6, D7) are connected to gates to form timing circuits.

The counter 74HC4060 (see Fig. 9.5.1 - 2 below) is connected to an RC element which fixes the frequency of the internal oscillator. An internal series circuit comprising 14 flip-flops is connected to the oscillator. If the memory formed by the two NAND gates ahead of the counter is in the reset state, a high is present at the reset input of the counter which switches all flip-flops to low. If the memory is set, then the reset input of the counter goes low, the oscillator turns on and after 2^{13} pulses a high is present at output Q14.

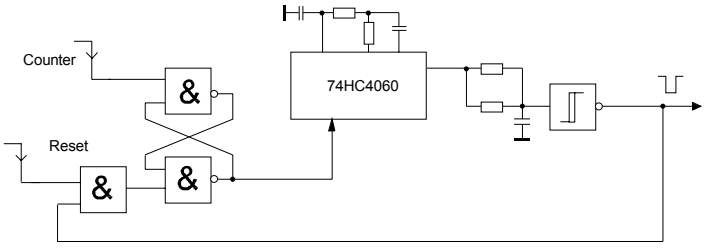

Fig. 9.5.1 - 2: Principle of the Timing Circuit

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The high acts to reset the counter (time delayed) through an RC element, an inverter and an AND gate. The charging- and discharging time constants of the RC element are different. The width of the reset pulse is determined by the dimensioning. Two timing circuits are incorporated in the reconnecting unit. In D7 the oscillator is set to a period of 0.34 ms, i.e., when counting, the output Q14 goes high after 2.8 s. In D6 the oscillator is set to a period of about 0.15 ms, i.e., when counting, the output Q14 goes high after about 2 minutes.

Fig. 9.5.1 - 3 shows a simplified block schematic of the reconnecting unit. If no faults are present, timers 1 and 2 (D7 and D6 respectively) and counter D8 are in the reset state. When a fault occurs a low signal is present at D18A and the output of D18B goes low. This activates the oscillator in timer 1. At the same instant the oscillator of timer 2 is activated via D18C and D18D.

Counter D8 is switched to high because the clock input is triggered to the negative going edge. After about 2.8 s output Q14 of timer 1 goes high. The pulse formed by the downstream RC element and inverter D22F is passed via D14D and D18B to reset the counter in timer 1 and output via D23C as the "Clear " pulse.

If a fault indication is no longer present at D18A after the "Clear" pulse then the counter in timer 1 remains in the reset state. If the fault indication is still present, the counter in timer 1 starts again and D8 counts one increment further. The fault indication also activates the counter in timer 2. Since the oscillator is set to a period of 15 ms the output Q14 of timer 2 goes high after 2 minutes. This resets counter D8 via D14B and D22B.

The counter in timer 2 is reset by the pulse formed by the downstream RC element and D22D through D14C and D18D. Counter D8 is a decimal counter with internal decoder. A number of the 10 outputs are connected to contact pins (X51...X54).

A jumper is used to set the desired number of "Clear" pulses and a line passes a "Continuous blocking" signal and a signal via D22C to reset the counters in timers 1 and 2 until D8 is reset by an external pulse.

Timer 2 has a time window function. It limits the number of "Clear" pulses given in 2 minutes. If this number is lower than that set by the jumper at D8 then timer 2 sets counter D8 to zero. If, on the other hand, the max. number of "Clear" pulses is output within the 2 minutes, then timers 1 and 2 are reset and the reconnecting unit goes into the state of "Continuous blocking".

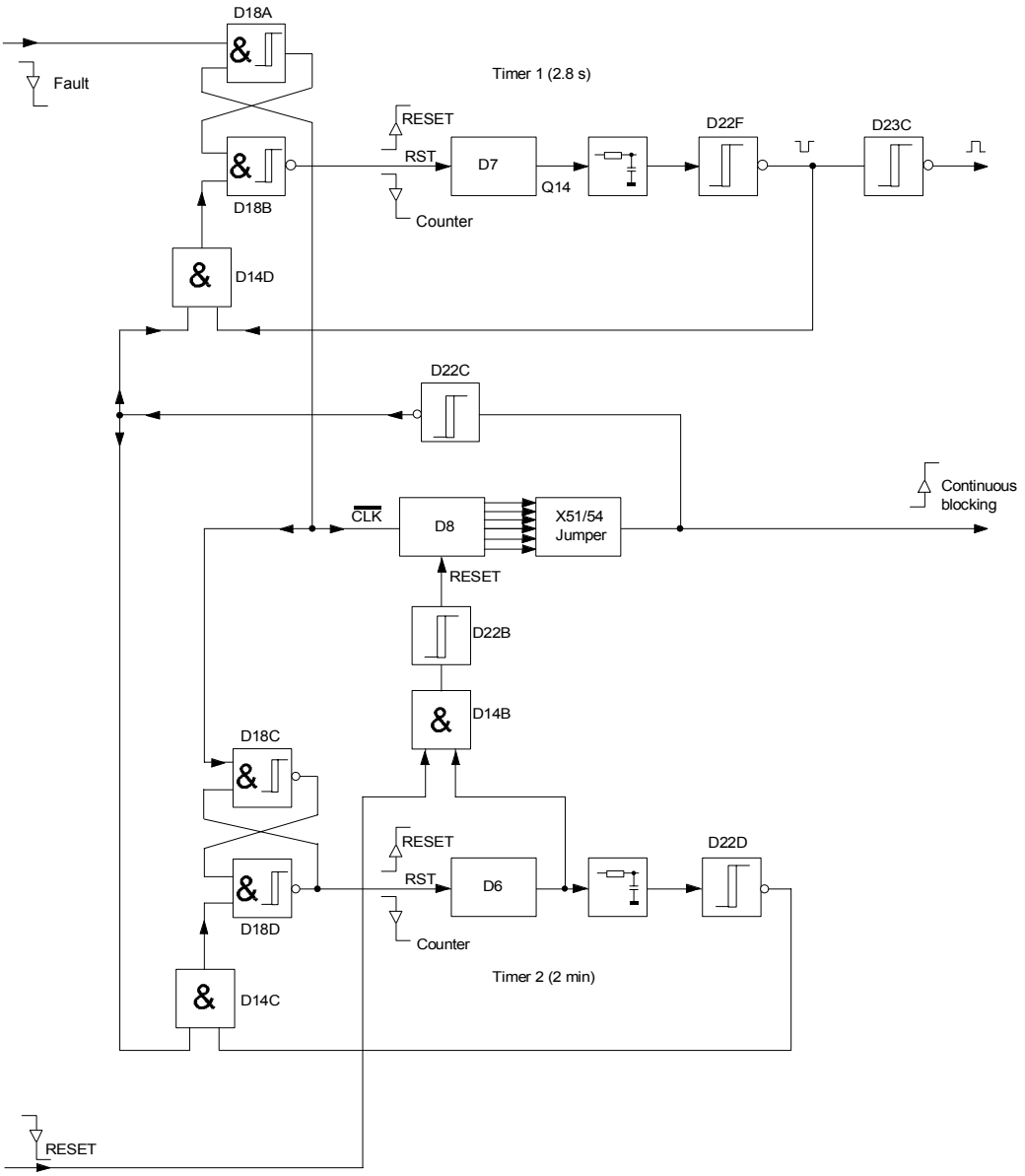

Fig. 9.5.1 - 3: Simplified Block Schematic of the Reconnecting Unit

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10 MONITORING THE INPUT CIRCUIT / POWER SUPPLY

10.1 Temperature of the Charging- and Discharging Resistors

The temperature of the charging resistors R8110, R8120 and R8130/R8150, R8160 and R8170 and the discharging resistors in the discharge circuits of the amplifier cabinets is monitored by PTC resistors. If the temperature is too high, for example, after repeated fast transmitter on-off switching, the control board inhibits further switching on of the transmitter until the temperature has dropped. Fault evaluation is by means of comparator D3/2 (see drawings 51-1584-121-00 WSP).

10.2 Temperature of the Transformer

The temperature of the windings of the transformers T 5400 in both amplifier cabinets is also monitored by PTC resistors. If the temperature is too high, the transmitter is switched off by the action of the control board. Transmitter restart is inhibited until the temperature has dropped sufficiently. Fault evaluation is by means of comparator D2/2 (see drawings 51-1584-121-00 WSP).

10.3 Temperature of the Rectifier Board

The temperature of the rectifier on boards A4050 and A4070 in the amplifier cabinets is monitored by PTC resistors mounted on heat sinks. If the temperature is too high, the transmitter is switched off by the action of the control board. Transmitter restart is inhibited until the temperature has dropped sufficiently. Fault evaluation is by means of comparators D2/3 and D2/4 (see drawings 51-1584-121-00 WSP).

10.4 Air Temperature

The air temperature is monitored by means of a thermal switch mounted on the PC boards of the discharge circuits in the amplifier cabinets. Above 50°C its contact opens and transmitter shutdown is initiated via comparator D3/1 (see drawings 51-1584-121-00 WSP).

10.5 Automatic Cutouts

The auxiliary contacts of all three automatic cutouts Q6100, Q6200, Q6500 and motor circuit breaker Q6300 are connected in series. If a cutout fails, the transmitter is switched off. Fault evaluation is by means of comparator D3/3 (see drawings 51-1584-121-00 WSP).

10.6 Monitoring the Supply Voltage U_0 (+270 V)

The voltage divider for the supply voltage is located in the discharge circuit (see drawing 51-1584-240-00 WSP). The monitoring voltage required by the control board is tapped at resistor R38 and evaluation is by means of measuring amplifier N4 and comparators D1A and D1B. The supply voltage for both amplifier cabinets is displayed by meter P20 in the control panel using the amplifier cabinet selector switch S1.

Under low voltage conditions (<250V) the PDM pulses in the preliminary stage are blocked by the action of D1B, D21A, and D9C in the cabinet monitors. Under overvoltage conditions (> 310 V) D1A, D9A and V107 in the cabinet monitors act to cause N4, D1A and D9A in the control board to respond thus initiating PDM blocking and transmitter shutdown.

10.7 Monitoring the Rectifier Current I_0

The rectifier current is passed through current transformers U5600 (1:2000) in the amplifier cabinets. The voltage drop across the terminating resistors of the current transformer (R20...R37 on the discharge circuit PC board 51-1584-240-00) is evaluated in the control board by measuring amplifier N5 and D1C and displayed by meter P30 in the control panel using the amplifier cabinet selector switch S2 for the respective amplifier cabinet. Under current conditions (I > 275A) D1C, D9B and V33 in the cabinet monitors act to cause N5, D1C and D9B in the control board to respond thus initiating PDM blocking and transmitter shutdown.

10.8 Mains Monitor

When the Mains monitor responds, the transmitter is switched off. Fault evaluation is by means of comparator D4B in the control board.

11. MONITORING THE FUNCTIONING OF THE RF PREDRIVER

see also drawing 51-1585-120-00

The RF predriver is equipped with a number of protective circuits which block the RF signal path and/or the PDM signal path to prevent a fault, e.g., voltage failure, from causing damage to components. In both cases, blocking leads to a loss of the RF output signal and thus to a transmitter shutdown.

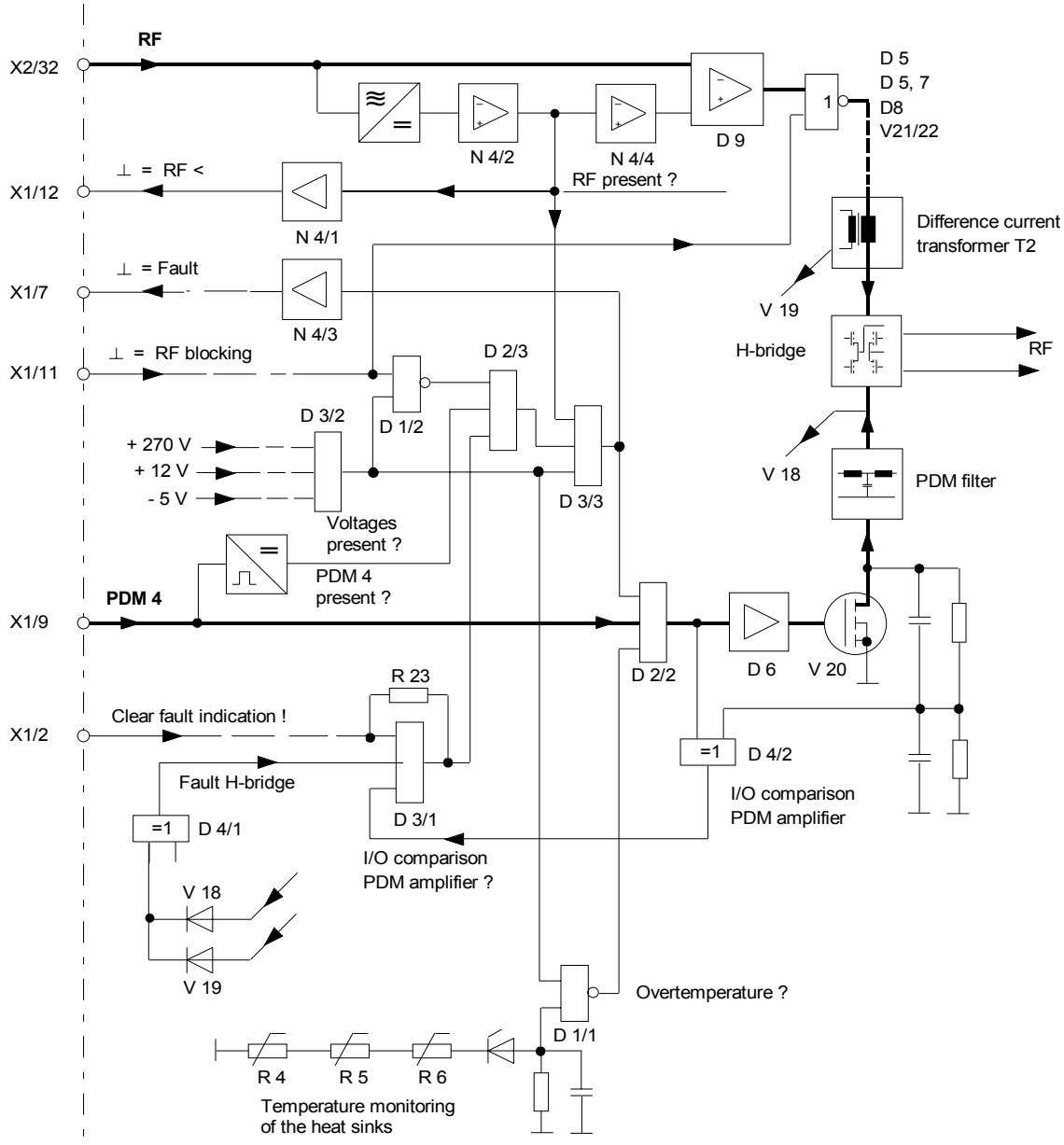

Fig. 11 -1: Simplified Block Schematic of the Monitoring Logic

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11.1 Criteria for the Blocking of the RF Signal Path

The criteria for the blocking of the RF signal path are; insufficient amplitude of the RF input signal or an "RF Blocking" signal from the transmitter control board.

In the first case, the RF signal path is blocked at the second input of comparator D9 by means of an offset voltage. In the other case, the RF signal path is blocked via gates D5/1 and D5/2.

11.2 Criteria for the Blocking of the PDM Signal Path

The criteria for the blocking of the PDM signal path are:

1. Operating voltage and/or auxiliary voltage(s) missing,
2 Amplitude of the RF input signal too low,
3. Overtemperature at the heat sinks,
4. Signal "RF Blocking" is present,
5. Fault in the PDM amplifier (I/O-comparison),
6. Fault in the RF amplifier (H-Bridge).

Blocking of the PDM signal path occurs through the action of gate D2/2. If blocking is initiated due to a "Fault in the PDM amplifier" or due to a "Fault in the RF amplifier" then these indications are stored in gate D3/1 because of the danger of follow-on faults. A transmitter restart in this case does not take place automatically but only after the stored fault indications are cleared.

11.3 Monitoring the Supply Voltage and the Auxiliary Voltages

Monitoring of the +270 V supply voltage, the +12 V auxiliary voltage and the -5 V auxiliary voltage (passed first through exclusive OR-gate D4/4) is by means of AND-gate D3/2. If one of the voltages is missing then the PDM signal path is blocked by the action of gates D3/3 and D2/2.

If the +5 V auxiliary voltage is not available then the complete CMOS logic will fail. The failure is captured by comparator N4/3 and passed to the control board as a fault indication. However, a necessary condition for this to occur is the presence of the +12 V auxiliary voltage. If the +5 V and +12 V auxiliary voltages fail then it is not possible to issue a fault indication.

11.4 Monitoring the RF Input Signal

The RF input signal (its amplitude should be in the range 1 V ±10 dB) is monitored by comparator N4/2. When the signal is missing or the amplitude too low, the rectified RF voltage at comparator N4/2 drops below a threshold value. N4/2 switches and blocks the PDM signal path via D1/4, D3/3 and D2/2 and at the same time blocks the RF signal path via N4/4 with an offset voltage applied to RF comparator D9. The signal "RF too low" (RF <) is passed to the control board by the output (switched to ground) of N4/1. The comparator N4/2 possesses regenerative feedback coupling (hysteresis) to prevent unstable operating conditions in the range of the threshold value.

In order to drive the RF amplifier (H-bridge) the RF input signal must be amplified. Amplification is handled (among other components) by comparator D9. The comparator switches during each zero cross-over of the RF input signal and therefore generates two square-wave form signals in phase opposition. The output signals have an amplitude of approx. 5 V. Variations in the RF input amplitude are thus corrected. If, however, the RF input amplitude takes on a value which does not ensure proper switching of comparator D9 then an offset voltage is applied to the second input of the comparator which causes it to block. This offset voltage is produced by device N4/4 used to monitor the amplitude of the RF input signal.

11.5 Monitoring the Power Transistors and Other Components

The power transistors are mounted on heat sinks employing temperature monitoring devices in the form of PTC resistors. If the temperature of a heat sink rises above a certain permissible value, the resistance of the respective PTC resistor goes high and the PDM signal path is blocked by the action of gates D1/1 and D2/2. The monitored components and the assigned PTC resistors are:

PTC Resistor R4	FETs V23, V24, V25 and V26 of the RF Amplifier
PTC Resistor R5	Voltage Regulators N2 (-5 V) and N3 (+12 V), FETs V21, V22 of the RF preamplifier
PTC Resistor R6	Voltage Regulator N1 (+5 V), FET V20, Commutating Diode V16

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11.6 Monitoring the RF Amplifier (H-Bridge)

The RF amplifier is monitored by the exclusive OR-gate D4/1 which evaluates measured values from the drive circuit for the H-bridge and also rapid changes in operating voltage at the H-bridge, e.g., due to a short in one of the bridge FETs. If a fault condition arises, D4/1 initiates blocking of the PDM signal path via gates D3/1, D2/3, D3/3 and D2/2. The fault indication is stored by gate D3/1.

The drive for the RF amplifier is monitored by measuring the drive currents. The drive currents are measured by the difference current transformer T2 which is looped into the supply lines to transformers T3 and T4 driving the FETs of the H-bridge. Faults are determined by a comparison of the drive currents. If a FET fails due to a gate-source short then a high voltage is induced at the secondary of T2 and at R65 (the load resistor of the current transformer). This voltage is rectified by V19.

If a FET of the H-bridge fails due to a drain-source short, then, because of the resulting high short circuit currents in the H-bridge, steep edged high voltage changes are induced at the output of the PDM filter. These are evaluated by the difference circuit C54, R67, R66 and rectified by V18.

Diode V7 protects the input side of gate D4/1 against overvoltages.

11.7 Monitoring the PDM Amplifier

The PDM amplifier is monitored by comparing the input signal with the output signal at V20. If PDM operation is fault-free, both signals are equal, however, phase shifted by 180°. If a fault occurs, the exclusive OR-gate D4/2 responds. The PDM signal path is blocked via gates D3/1, D2/3, D3/3, and D2/2 and the fault indication is stored in gate D3/1.

11.8 Storing and Clearing Fault Indications

The indications "Fault in the RF amplifier" and "Fault in the PDM amplifier" are stored in gate D3/1 by feeding the gate output signal (logical 0) through resistor R23 back to one of the gate inputs. The stored fault indications can only be cleared when fault signals are no longer present. A "Clear" command in the form of a short switching edge at X1/2, either positive (0 V $\rightarrow$ 5 V) or negative (5 V $\rightarrow$ 0 V) is sufficient for this purpose. The exclusive OR-gate D4/3 generates from this edge a narrow positive pulse whose width is determined by the magnitude of R22 and C14. This positive pulse resets gate D3/1.

11.9 Signaling

Faults or problems associated with the RF driver are indicated by LEDs H1...H5 on the driver PC board and by LEDs on the control panel.

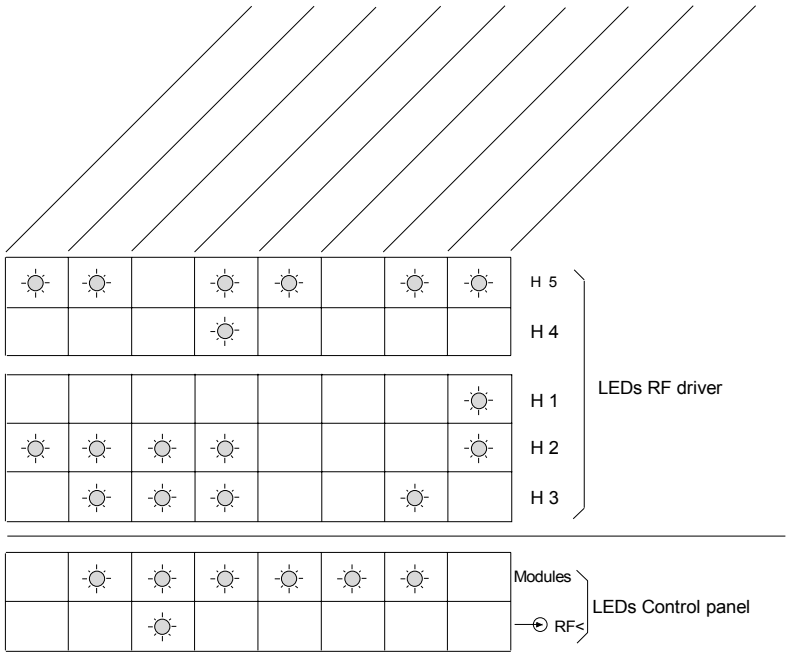

Fig. 11.9 - 1: Signaling LEDs at the RF Driver and in the Control Panel

12. MONITORING THE FUNCTIONING OF THE AMPLIFIER MODULE

see also drawing 51-1585-100-00 WSP

12.1 Monitoring the Operating Voltage and the Auxiliary Voltages

The operating voltage (+270V) and the two auxiliary voltages (+12V and -5 V) are monitored by AND-gate D1/2. If all three voltages are available, the output of the gate is high. A fault initiates PDM blocking via V16, D1/1 and D4/3. At the same time, a fault indication is passed to the control board via D3/4 and V13. All LEDs turn off. If the third auxiliary voltage (+5V) is missing then the CMOS logic fails and a fault indication is passed to the outside via V12 and V13. If the +5V and the +12V supplies fail it is no longer possible to pass a fault indication to the outside.

12.2 Monitoring the PDM Amplifier

The PDM switch (transistors V5/V6) is monitored by the exclusive OR-gate D2/2 by comparing the drive signal with the signal at the switch output. In fault-free operation, the output of gate D2/2 is high. A fault initiates PDM blocking via D1/3, V15, D1/1 and D4/3. At the same time, the fault is signaled by LED H3 via D1/1 and a fault indication is passed to the control board via D3/1 and V13. LED H2 turns off.

12.3 Monitoring the RF Amplifier (H-Bridge)

The H-bridge is monitored by the difference current transformer T2. A fault in the H-bridge produces a high voltage at R23 which is rectified by V22. In fault-free operation, the output of exclusive OR-gate D2/3 is high. A fault changes the logic state of D2/3 and leads to PDM blocking via D1/3, V15, D1/1 and D4/3. This condition is stored by D1/3. At the same time, the fault is signaled by LED H3 and a fault indication is passed to the control board via D3/4 and V13. LED H2 turns off.

12.4 Monitoring the Heat Sink Temperature

The MOSFETs of the H-bridge are mounted on a heat sinks equipped with PTC resistors for the purpose of temperature monitoring. PTC resistor R37 monitors the heat sink on which MOSFETs V26, V27 and V28 are mounted. PTC resistor R38 monitors the heat sink on which MOSFETs V35, V36 and V37 are mounted.

Furthermore, MOSFETs V5 and V6 of the PDM switch together with resistor R44 are mounted on a heat sink where temperature monitoring is by means of PTC resistor R36.

All three PTC resistors are connected in series and connected to inverter D3/3. The output of D3/3 is high when no overtemperature is measured. Under overtemperature conditions the respective PTC resistor has a high ohmic value and changes the logic state of D3/3. PDM blocking takes place via D4/3 and the fault condition is displayed by LED H1. PDM blocking remains only as long as the temperature is high and does not lead to an external fault indication. The signaling of overtemperature by means of H1 is independent of RF- and PDM monitoring.

12.5 Signaling

Three LEDs on the front side of each amplifier module indicate its current operating status:

H1 (yellow)	H2 (green)	H3 (yellow)	Meaning
●			PDM blocking due to overtemperature
○	○	○	Fault operating voltages
When H1 lights up: Pulse blocking	●	○	Operation
	●	●	Ready, however, PDM and/or RF missing
	○	●	Fault, PDM switch or H -bridge

Fig. 12.5 - 1: LEDs on the Front Side of the Amplifier Modules

Note: Under overtemperature conditions (H1 illuminated) pulse blocking always occurs independent of the respective operating state (standby or operation). The blocked pulses are automatically released when the temperature has dropped sufficiently. The indication "Overtemperature" is not passed to the outside.

13. MEASURING AND MONITORING THE RF OUTPUT SIGNAL

13.1 Monitoring the Tuning of the Output Filter

A discriminator is used to monitor the tuning of the output filter. To achieve high efficiency, the output load for the RF power amplifier must be slightly inductive. The phase of the load impedance is displayed by the phase meter.

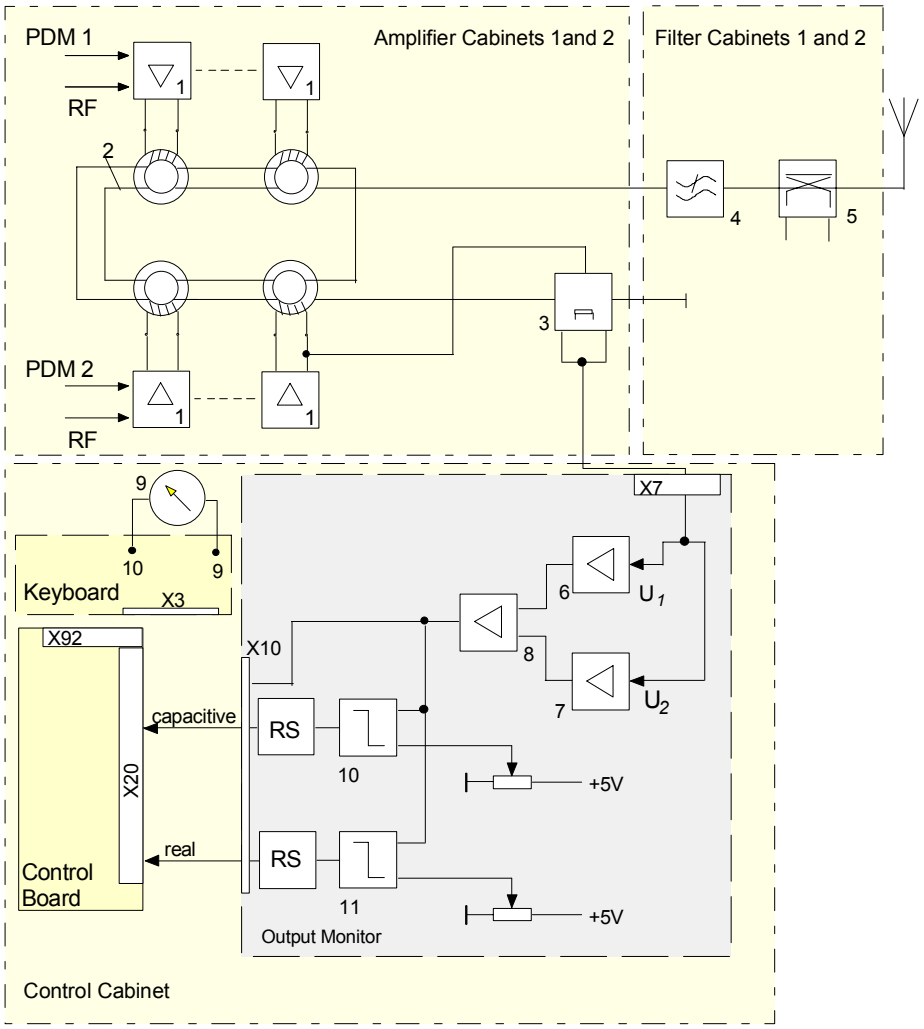

Fig. 13.1 - 1: Simplified Block Schematic to Monitor Output Filter Tuning

1	Amplifier modules		
2	Combiner assembly		
3	Discriminator		
4, 5	Filter and feed line monitor (FLM) in the control cabinet		
6,7,8	Op. amplifier	(6) N14, (7) N15, (8) N13	in the AF stage
9	Tuning meter P40		
10,11	Comparator	(10) N2A, (11) N2B	in the AF stage

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To determine the phase of the load impedance for the amplifier modules, a voltage proportional to the output voltage of the last amplifier module is coupled out by a capacitive voltage divider circuit in the discriminator [3]. A current proportional to the output current of the transmitter is coupled out through current transformer T1 (ahead of the output filter) in the discriminator. From these, the discriminator generates two voltages U_1 and U_2 which are evaluated in the output monitoring circuit.

The phase information is provided by amplifier [8] by forming the difference of both voltages U_1 and U_2. U_{diff} is displayed by the phase meter [9]. In addition, the difference voltage is monitored by two comparators [10], [11]. If the difference voltage is too high, e.g., capacitive loading of the power amplifiers, then the transmitter is either shut down [10] or a warning indication is passed to the control panel [11].

13.2 Discriminator

The discriminator [3] generates the voltages U_1 and U_2 required for further evaluation. Capacitive voltage divider C_a / C_b couples out a voltage U_{Uout} proportional to the output voltage U_{out} of the last amplifier module. Transformer T1 couples out a current I_{Iout} proportional to the output current I_{out}. I_{Iout} generates at the equal valued capacitors C_c and C_d a voltage U_{Iout} proportional to the output current I_{out} which, however, lags this by 90°.

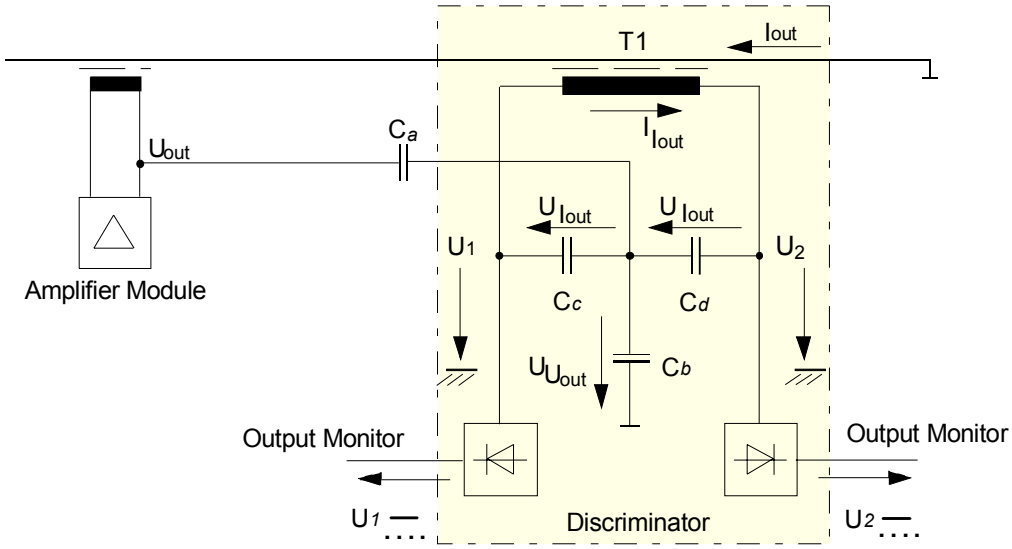

Fig. 13.2 - 1: Simplified Schematic of the Discriminator Circuit

U_1 and U_2 are generated by forming the sum and difference of U_{Iout} and U_{Uout}. The difference between U_1 and U_2 is a measure which determines whether the load for the RF power amplifier is capacitive or

inductive. From the vector diagram (see below) it can be seen that the voltages are of equal magnitude, when the current I_{out} and the voltage U_{out} are in phase.

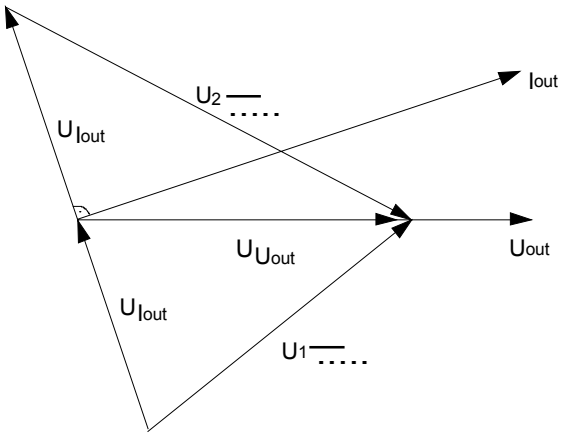

Fig. 13.2 - 2: Vector Diagram for Current and Voltage

13.3 Implementation

The capacitive voltage divider C_a / C_b consists of C1 and the selectable (by means of plug X5) parallel connection of C2 to C11 as well as C41 to C45.

The capacitance C_c and C_d is formed by capacitors C27 to C29, C35 to C37 and C47 + C48 respectively.

Alignment takes place in the factory taking into consideration the frequency and rated power.

The rectification of the high frequency sum- and difference voltage is by means of diodes V1, V2, V5 and V6 and V3, V4, V7 and V8 respectively. The downstream inductance's L9...L14 and L15...L20 together with capacitors C14, C15 and C16, C17 serve to suppress the high frequency components remaining after rectification.

The voltages U_1 and U_2 at the output of the discriminator are balanced.

Evaluation

The balanced voltages U_1 and U_2 are applied to input amplifiers N14 [6] and N15 [7] in the output monitor and converted to unbalanced voltages. The downstream amplifier N13 [8] forms the difference of both voltages which is a measure for the phase of the load impedance of the RF power amplifier.

The negative voltage generated with inductive loading is displayed by phase meter P40 [9] in the front panel of the transmitter.

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In addition to the display, the difference voltage is evaluated by comparators N2A [10] and N2B [11].

If the load impedance is real, comparator [11] switches and a warning indication is signaled in the control panel.

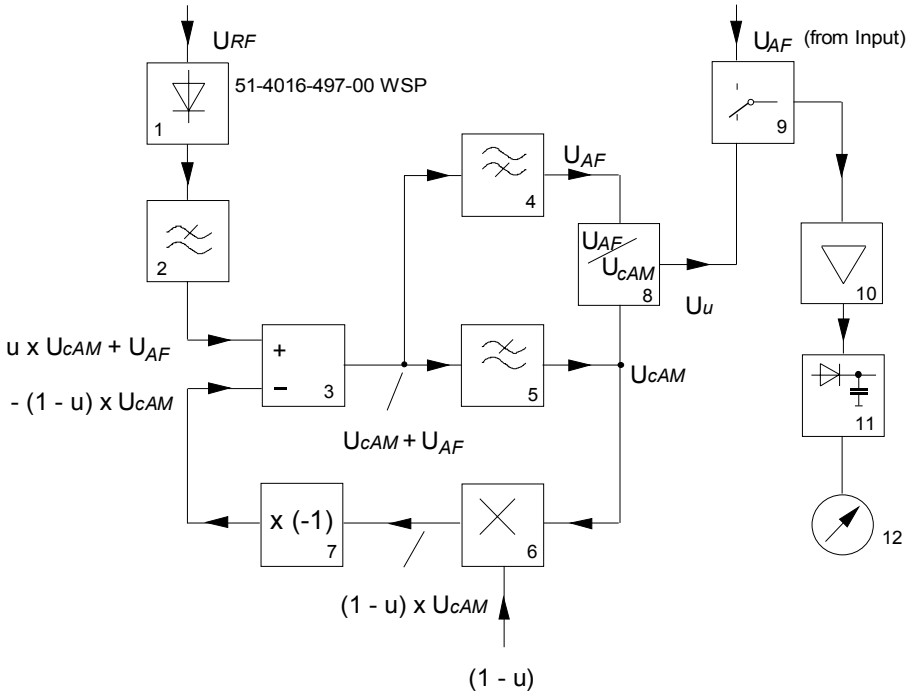
LED H21 lights up.

If the load impedance is capacitive, comparator [10] switches and transmitter shutdown is initiated with restart trials.

LED H39 in the control panel lights up.

13.4 Determining the Modulation Factor "M" and Modulation "U"

The RF voltage is tapped behind the harmonic filter at the transmitter output by a C-R voltage divider, rectified by a demodulator [1] and passed through the downstream low-pass filter [2] to separate out residual components of the RF carrier voltage. The output of the low-pass filter thus provides a dc voltage $u \times U_{cAM}$ (U_{cAM} = carrier voltage in AM operation) proportional to the carrier voltage, which is superimposed with the AF modulation voltage U_{AF} when the carrier is modulated. Dividing the AF modulation voltage by the dc voltage proportional to the RF carrier in [8] gives the value "u" for the modulation. The separation of ac and dc voltage components, required for division, takes place through a high-pass [4] and a low-pass filter [5].



[1]	Demodulator	[8]	Divider
[2]	Low-pass filter	[9]	Switch (Relay)
[3]	Comparator	[10]	Amplifier
[4]	High-pass filter	[11]	Peak value rectification and storage
[5]	Low-pass filter		
[6]	Multiplier	[12]	Modulation meter
[7]	Sign reversal		

Fig. 13.4 - 1

The value "u" for the modulation corresponds, in AM operation, to the modulation factor "m". In DAM operation, however, a smaller dc voltage component is present as a result of carrier reduction in the middle modulation range (refer to Fig. 6.1.1-2 DAM Characteristic Curve - in Section 6.1.1). This has the effect of producing a higher modulation factor "m" compared to AM operation with the same AF modulation.

In order that the modulation meter [12] indicates the same value in AM- as well as DAM operation at the same modulation "u", the smaller dc component present at the output of the demodulator during DAM is raised in value by a compensating circuit [6] + [7] to give the correct magnitude for the divider.

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The output signal U_u of the divider [8] is amplified [10] and applied to the downstream peak value rectifier and storage circuit [11] so that the value for the modulation "u" (in AM mode "u" = "m") can be read at the modulation meter.

All functional groups for the evaluation of the RF voltage tapped by means of the C-R voltage divider are located in the assembly "AF stage".

Demodulator [1]

The demodulator incorporates a voltage doubling circuit to provide rectification. The RF input is terminated with 50 Ω.

Low-pass Filter [2]

The frequency limit of the active low-pass filter N26 is approx. 65 kHz, the attenuation at 500 kHz is around 50 dB.

Compensating Circuit [3], [6], [7]

The difference amplifier N331 is connected ahead of the low-pass filter [5] N318. It compares the demodulated RF voltage u x U_{cAM} + U_{NF} with a reference voltage -(1-u) x U_{cAM}, formed by multiplication of the output voltage of N318 with a voltage derived from the carrier control circuit (N8 / N9). Multiplication takes place with device N321 and sign reversal with N329.

In DAM operation, if the dc component at the "+" input of the difference amplifier is reduced, then the reference voltage at the inverting input of the amplifier is altered by the same amount, so that the dc component at the output of the amplifier (or at the output of the low-pass filter N318) remains constant. If the output voltage is correctly set with R377, no voltage jumps occur when switching from AM to DAM operation. Consequently, at the same modulation, the modulation meter shows the same value for both operating modes, whereby in AM mode the modulation factor "m" and in DAM mode the modulation "u" is displayed.

High-pass Filter [4], Low-pass Filter [5], Divider [8]

The separation of the AF modulation voltage and the dc voltage proportional to the carrier, required for division, takes place through the action of the high-pass (C343/N319) and the low-pass (N318) filters. The low-pass filter has a limiting frequency of about 3 Hz.

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The divider N323 forms the quotient out of the ac- and dc voltages. At a modulation factor m = 1, the output voltage U_u at N326 is set to +6 dBm with potentiometer R326. With this setting the modulation meter P50 shows 100%.

When the transmitter is switched off, the demodulator does not provide an output voltage so that a division by zero would result in N323. To avoid an undefined output voltage at N326, FET V313 applies a dc voltage to the input of the low-pass filter N318 in case the demodulator output voltage is missing.

The presence of a demodulator output voltage is evaluated by comparator N310 by measuring the output voltage at N26 ($U \geq 0.4V$).

Peak Value Rectification and Storage [10], [11]

Amplifier N27 serves as a level matching device since the peak value rectifier requires a drive signal as high as possible to keep offset errors small.

The circuit downstream of amplifier N27 provides peak value rectification and storage with a defined holding time. The holding time is determined by the retiggerable one-shot multivibrator D2. The multivibrator is triggered by the positive edge of the output voltage of comparator N28, which compares the instantaneous value of the test voltage (= output voltage at N27) with the output voltage of amplifier N29. After a delay time fixed by R223 and C207, the output $\overline{Q}$ of D2 switches, transistor V208 conducts and capacitor C206 is discharged through resistor R225. When the instantaneous value of the test voltage again rises in comparison to the output voltage at N29, the output voltage of comparator N28 is again positive, D2 is triggered, transistor V208 blocks and capacitor C206 is recharged with a very small time constant through R228 and V207.

13.5 Determining the Output Power "P" and the Mismatch "S"

The output power P_o and the mismatch s are determined by coupling out two voltages $U_{forw.}$ and $U_{refl.}$ through the feed line monitor located behind the output filter. These voltages are proportional to the forward and reflected wave of the output signal. Both voltages are evaluated by the output monitor in the control cabinet.

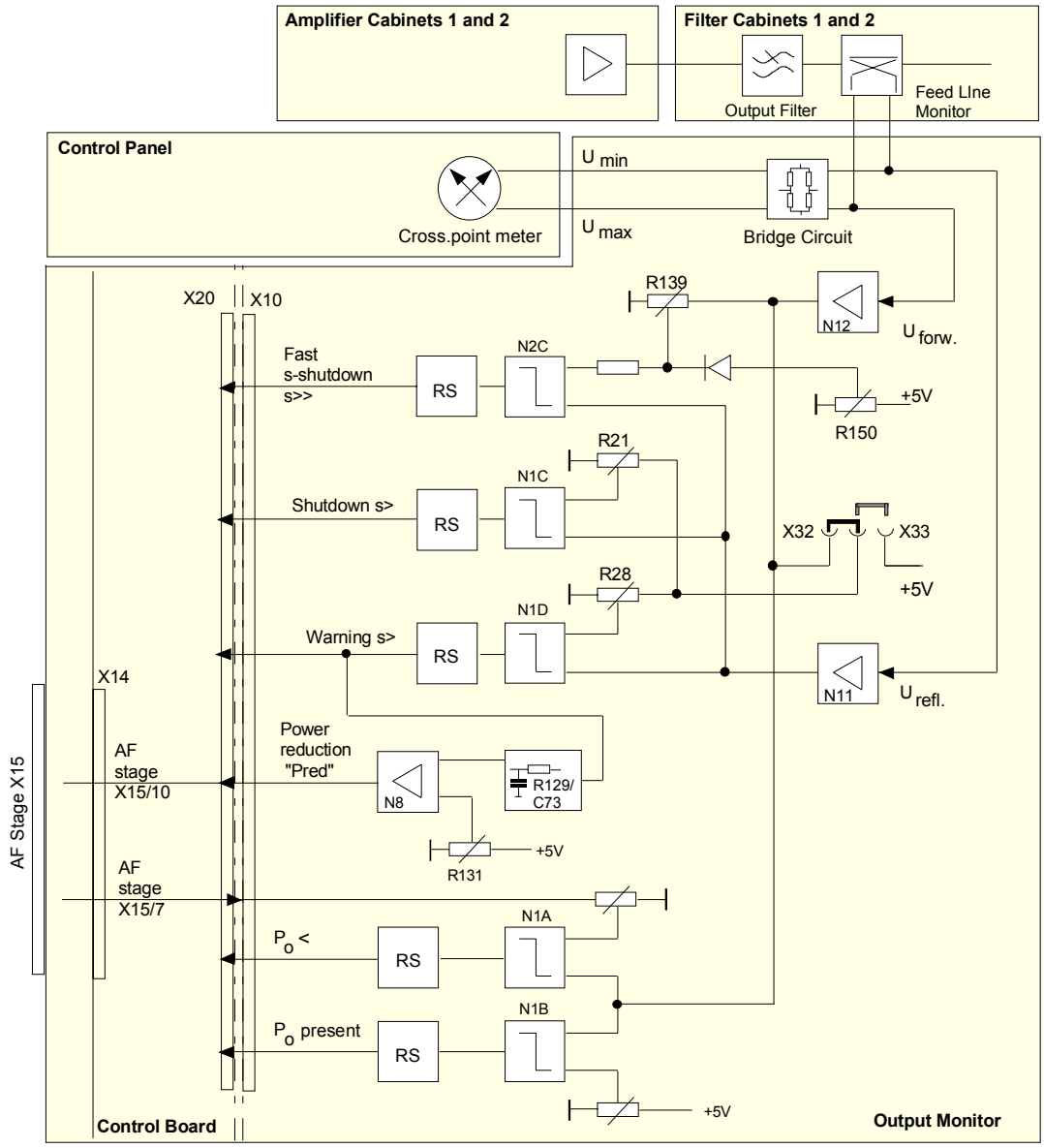

Fig. 13.5 - 1: Simplified Block Schematic of the Output Monitoring Circuit

The voltages U_{max} and U_{min} are produced by forming the sum and difference of the forward and reflected voltages in a bridge circuit.

$$U_{max} = U_{forw} + U_{refl} \qquad U_{min} = U_{forw} - U_{refl}$$

U_{max} and U_{min} are displayed at the cross-point meter such that at the crossing of both pointers the output power P_o and the mismatch s can be read off from the scale.

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Comparators N2C, N1C, N1D, N1A and N1B compare the voltage U_{refl} with a reference voltages derived from the 5 V control voltage or from U_{forw} and are therefore dependent of the output signal of the transmitter. If the comparators respond, then this leads to the implementation of protective measures for the transmitter. These may involve a reduction in output power or transmitter shutdown.

13.6 Feed Line Monitor

The feed line monitor couples out through the capacitive voltage divider C_a / C_b a voltage U_{Uout} proportional to the output voltage U_{out}. Current transformer T1 couples out a current I_{Iout} proportional to the output current I_{out} which generates, across the equal valued resistors R_a and R_b, a voltage U_{Iout} proportional to the output current I_{out}.

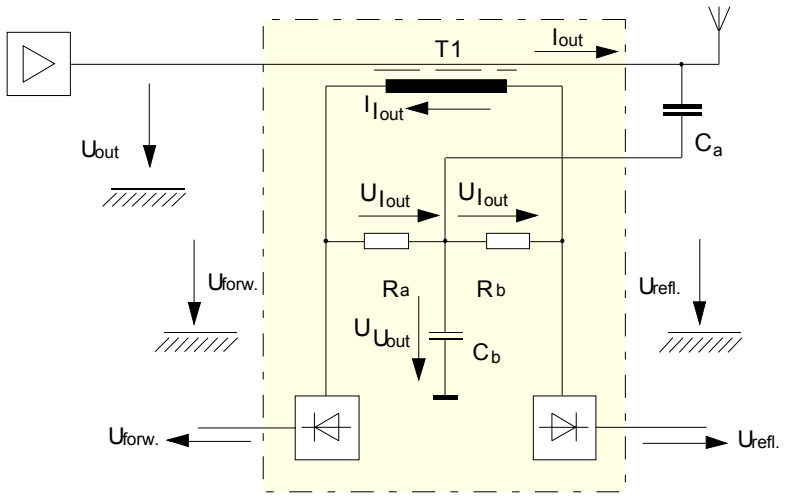

Fig. 13.6 - 1: Basic Principle of the Feed Line Monitor

From general principles concerning current and voltage on a line with a characteristic impedance Z_L one can derive the following relationships:

The voltage at an arbitrary point on the line is the sum of the forward- and reflected voltages:

1.) $U = U_{forw} + U_{refl}$

The current at an arbitrary point on the line is the difference of both currents:

2.) $I = I_{forw} - I_{refl}$

For both waves the following applies:

3.) $U_{forw} = Z_L * I_{forw}$ and $U_{refl} = Z_L * I_{refl}$

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2.) and 3.) gives:

4.) $Z_L * I = Z_L * I_{forw} - Z_L * I_{refl} = U_{forw} - U_{refl}$

5.) $Z_L * I = U_{forw} - U_{refl}$

Adding 1.) and 5.) gives:

6.) $U + Z_L * I = 2 * U_{forw}$ or $U_{forw} = 0.5 * (U + Z_L * I)$

Subtracting 1.) and 5.) gives:

7.) $U - Z_L * I = 2 * U_{refl}$ or $U_{refl} = 0.5 * (U - Z_L * I)$

with $U = U_{Uout}$ and $Z_L * I = U_{Iout}$ one obtains:

8.) $U_{forw} = U_{Uout} + U_{Iout}$ and $U_{refl} = U_{Uout} - U_{Iout}$

The resistor R_a is formed by resistors R1 to R6 connected in parallel. R_b is formed by resistors R7 to R12.

The capacitive voltage divider C_a / C_b consists of C1 and the selectable (by means of a jumper) parallel connection of C2 to C11.

Alignment occurs during testing of the transmitter in the factory.

The voltages U_{forw} and U_{refl} at the output of the rectifier in the feed line monitor are balanced.

The diodes V1, V2 and V3, V4 rectify the coupled out high frequency voltage. The low-pass filters, consisting of C18, C19, L9...L14, C14, C15 and C20, C21, L15...L20, C16, C17 respectively, serve to suppress the remaining high frequency components after rectification.

13.7 Bridge Circuit

(see drawing 51-1584-140-00 WSP)

The bridge circuit in the output monitor generates from the voltages U_{forw} and U_{refl} the voltages U_{max} and U_{min} which feed the cross-point meter.

$U_{max} = U_{forw} + U_{refl}$ $U_{min} = U_{forw} - U_{refl}$

The currents resulting from the voltages U_{forw} and U_{refl} add in resistors R25 and R23, and are subtracted from another in R26 and R20. Thus the voltages U_{max} and U_{min} at resistors R25 and R26 are proportional to the sum and difference of U_{forw} and U_{refl}.

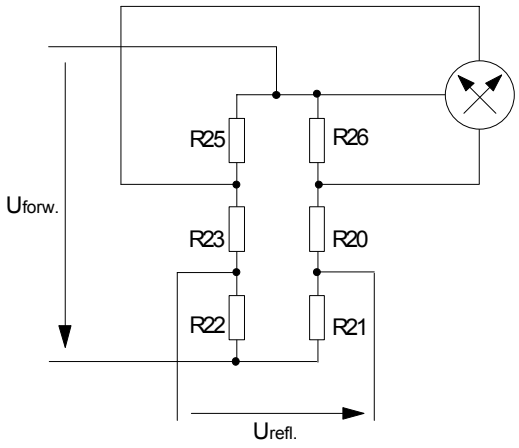

Fig. 13.7 - 1: Bridge Circuit

The output voltages of the bridge circuit therefore correspond to the maximum and minimum voltages on the feed line. At the crossing of both pointers one can read the output power P_o and the mismatch "s" from the scale.

13.8 Conditioning the Voltages $U_{forw.}$ and $U_{refl.}$ for further Evaluation

The balanced voltages U_{forw} and U_{refl} delivered by the feed line monitor are applied to input amplifiers N12 and N11 in the output monitor and converted to unbalanced signals for further evaluation.

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13.9 Fast "s"-Shutdown

In order to protect the antenna feed line and the antenna, a fast transmitter shut down is initiated, without preceding power reduction, when the mismatch is about s ≥ 1.5. The evaluation of the voltage U_{refl} occurs with comparator N2C by comparing this voltage with the reduced voltage U_{forw} set with potentiometer R139. This reduced voltage corresponds exactly to the value of the voltage U_{refl} up to the point where no fast shut down due to mismatch is necessary.

The downstream RS-flip-flop D34A and D34B stores the fault indication. The indication is cleared with each transmitter restart trial via the reconnecting unit in the control board. If after a set number of trials transmitter switch-on is not successful then transmitter remains in the OFF state. The fault indication can now only be cleared by pressing the "Clear" key S14 in the control panel of the transmitter.

Potentiometer R150 is used to set a voltage which simulates U_{forw} to ensure that the comparator does not respond when the transmitter is switched off and the voltages U_{forw} and U_{refl} are missing.

13.10 Warning and Power Reduction under Excessive Mismatch Conditions

When mismatch slowly increase, e.g., during progressive ice formation on the antenna, an attempt is made to continue service at reduced power.

The evaluation of the voltage U_{refl} occurs with comparators N1C and N1D. Here, for the reference voltage, the possibility presents itself of selecting a voltage dependent on U_{forw}, i.e., a voltage proportional to the output voltage of the transmitter or a fixed set voltage. In the second case a maximum permissible voltage is used as the switch-off threshold without reference to the output voltage of the transmitter. Here, selection is made by placing the shorting plug at X33.

If the threshold set with R28 is exceeded, comparator N1D switches, the warning indication is not permanently stored in the downstream RS-flip-flop. The flip-flop is reset as soon as the switching threshold at N1D is again below the set value. This is achieved by applying zero potential via connection X3/X25 to the respective input of the flip-flop. The warning indication is signaled by a LED in the control panel of the transmitter.

At the same time as the warning indication is present, the output signal of amplifier N8 (via timing element R129/C73) affects the duty factor of the pulses "PDM 1" and "PDM 2" processed in the AF stage so that the output power of the transmitter is reduced. In fault-free operation, potentiometer R131 sets a reference value for the output power. If the RS flip-flop is set, the voltage at capacitor C73 increases and the output power is reduced as a function of the changing reference value.

If mismatch increases further, transmitter shutdown occurs through the action of comparator N1C and the downstream RS-flip-flop in similar fashion as fast s-shutdown. The shutdown threshold is set with R21.

13.11 Monitoring the Output Power

The voltage U_{forw} is compared in comparator N1A with a voltage derived from a control voltage for the output amplitude generated in the AF stage (terminal X15/7). This ensures that when operating with wanted reduced power or in DAM mode, the comparator does not switch (respond). It only switches when U_{forw} deviates from the value determined by the AF stage. The output power also drops when several power modules fail (this however, only results in the warning indication "Module Fault" being issued) or a flashover occurs in the output filter or combiner.

Comparator N1B monitors the presence of a minimum output power.

Strictly speaking, in the above description of the monitoring of output power, the voltage corresponding to the forward wave of the transmitter output signal is monitored. In normal operation and with a sufficiently small antenna mismatch a sufficiently accurate value for the output power may be assumed.

14. PREPARING FOR OPERATION

The work to set the transmitter up for operation must be performed by qualified technicians.

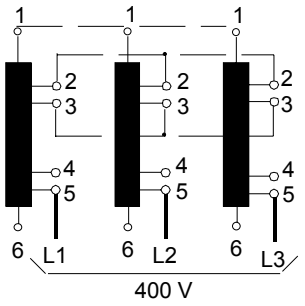
The transmitter has been tuned in the factory to the operating frequency of f_0 = 954 kHz. A new frequency alignment is not required. It is only necessary to check the factory measured values.

The prerequisite for preparing for operation is that the transmitter is completely and correctly installed.

Loadbreak switch Q6000 at the lower front of the control cabinet must be disengaged (lever in horizontal position).

14.1 Checking Mains Power Connection

The transmitter is factory set to a phase voltage of 400 V.



Star point connection	Primary voltage terminal	V
U 1 - 1 - 1	6	440
	5	426
V 2 - 2 - 2	6	413
	5	400
W 3 - 3 - 3	6	387
	5	374
	4	360

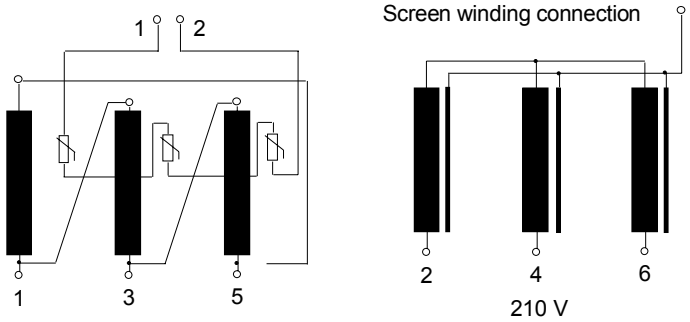


Fig. 14.1 - 1: Transformer Tappings for 400 V

Connect the 230 V feed for the auxiliary voltage power supply unit (assembly A3200 in the control cabinet) to terminal X1/X2 of this assembly as shown in Fig. 14.1 - 2 below. The phase-to-phase mains voltage is 400 V, 50 Hz.

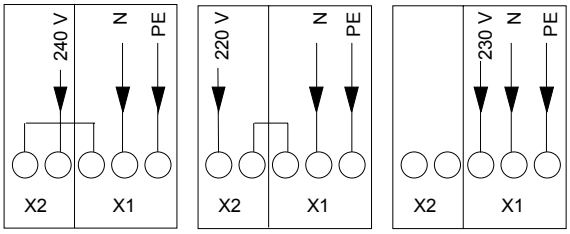


Fig. 14.1 - 2: Connecting Scheme for 230 V feed for the Auxiliary Voltage Power Supply Unit

Preparing for operation is described below with reference to Fig. 14.1 - 3 which shows, in simplified form, an example of the essential connection of a low voltage distribution for the transmitter.

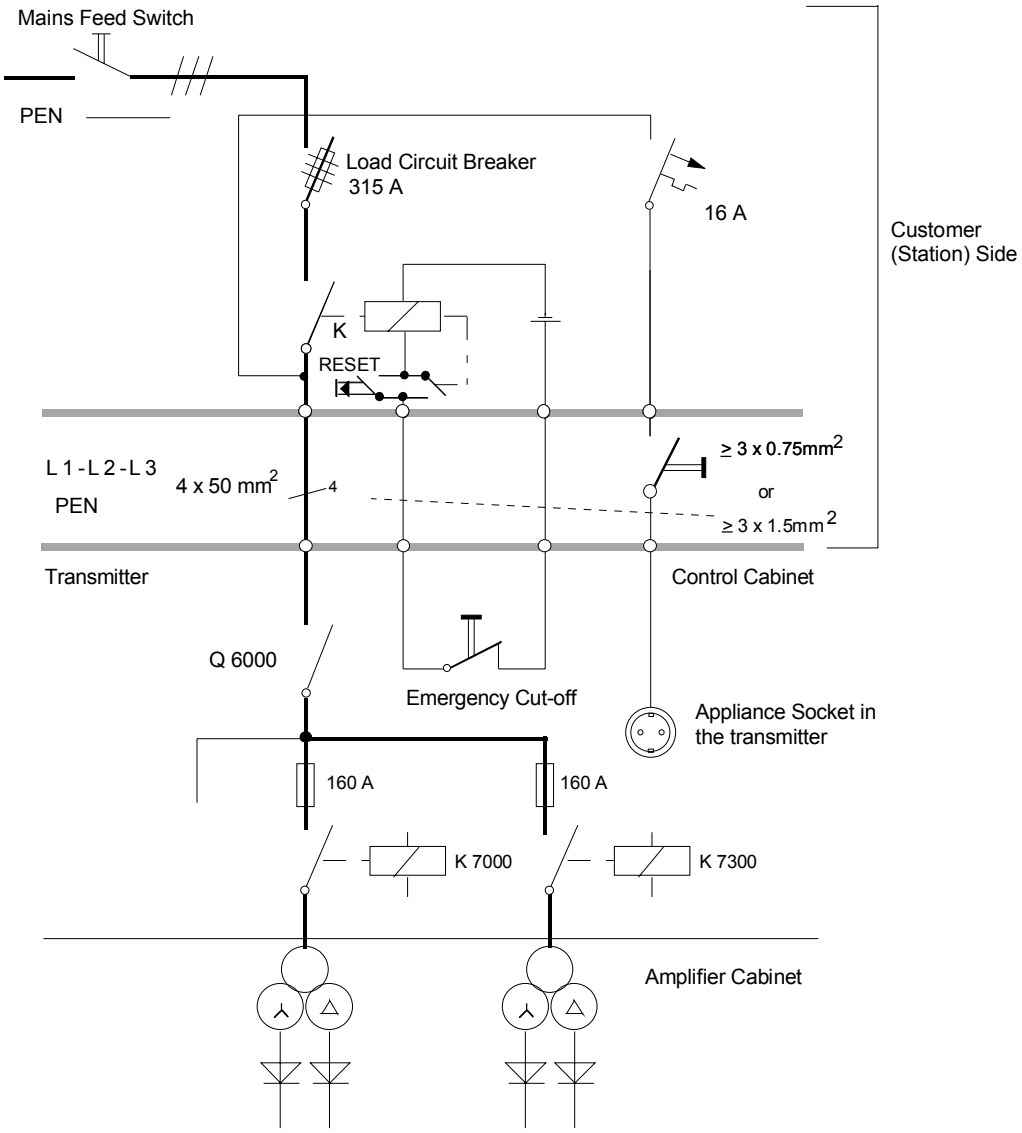


Fig. 14.1 - 3: Principle of a Low Voltage Distribution

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All safety switches (circuit breakers) in the station low voltage distribution must be switched off:

- Load circuit breaker for the transmitter (315 A),
- Automatic cutout (16 A) for the emergency cut-off loop
- Fuse switch (16 A) for the appliance socket in the transmitter

Press the emergency cut-off button (= cut-off position).

Engage the mains feed switch on the station side for the low voltage distribution.
Engage the automatic cutout for the emergency cut-off loop.

- Main contactor (K) in the station low voltage distribution must not pick up.

Unlocking the emergency cut-off button: Remove the transparent cap (snap-action lock), pull out the button until it indents in the end position and then replace the cap.

- Contactor (K) in the station low voltage distribution must pick up when the RESET button is pressed.

Engage the fuse switch for the appliance socket.

- Check the presence of power at the transmitter appliance socket and check for proper connection using a voltage tester.

Engage the load circuit breaker (315 A) for the transmitter in the station low voltage distribution.
Remove the AF input patch plug from the transmitter control panel to prevent the unintentional application of a modulation signal.
Disconnect the PDM lines at connectors X4, X5, X6 and X7 in the AF stage to prevent an unintentional release of PDM pulses and thus power.

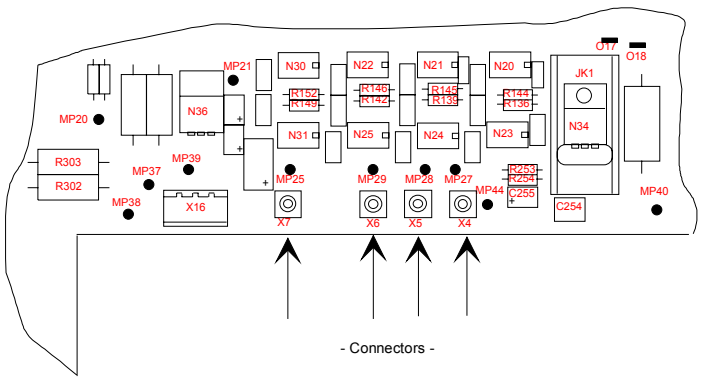

Fig. 14.1 - 4: Position of PDM Line Connectors in the Preliminary Stage

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Engage the loadbreak switch Q6000 at the lower front panel of the control cabinet.

- The transmitter cooling fans power-up.
- The following LEDs on the transmitter control panel light up (it may be that the corresponding keys have to be pressed when the transmitter is switched on for the first time):

	Designation	Symbol	Color
S3	OFF	O	green
S1	LOCAL		green
S8	AM	AM	green
S6	PDM OFF	O PDM	green
S10	Filter OFF	O 	green

- All fault indications (yellow LEDs) should be off with the possible following exception:

LED	Designation	Color	Meaning
H32	External carrier loop	yellow	external carrier blocking loop open

Press the emergency cut-off button at the transmitter.

- Contactor (K) in the station low voltage distribution drops out
- all displays at the transmitter turn off.
- no voltage is present at the transmitter

Unlock the emergency cut-off button:

- Remove the transparent cap (snap-action lock), pull out the button until it indents in the end position and then replace the cap.
- Press the reset button in the low voltage distribution
- The status of the transmitter before the emergency cut-off button was activated is again restored.

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14.2 Transmitter Switch-On

Connect the transmitter to the antenna or dummy load.

- External carrier loops must be closed.
- Yellow LED ”Ext. Carrier Loop” turns off.
- Press key S1 "Local".
- Enable the keys by placing slide switch S15 to the left.
- Press key PDM inhibit (O PDM) and press key AM.

Reconnect the PDM lines to the AF stage.

Press key "P2" (power stage 2). Power stage 2 is set to P_{RF} = 50 kW.

- Green LED in key "P2" lights up.
- Auxiliary contactors K7100, K7400 and main contactors K7000, K7300 in the control cabinet pick up.
- Green LED H16 ” I ” in the control panel lights up.
- Meter P20 displays a supply voltage between 270 and 300 V DC.

Press key ”PDM I”.

- The green LED in the key lights up.
- The green LED H15 ”PDM” in the control panel lights up
  when all conditions for PDM enable are satisfied.
- Only the green LEDs of all amplifier modules must be illuminated.
- The transmitter delivers 50 kW RF carrier power provided power reduction or transmitter shutdown does not take place due to too high VSWR. In this case the LEDs H22, H40 or H41 light up. At high deviation from the ideal value VSWR =1.0 the transmitter protects itself by reducing the RF output power or shuts down. If this occurs proceed as described under "Tuning the Transmitter " below.
- At the cross-point meter P10 read off the output power (horizontal line) and the mismatch (vertical line) at the position where both pointers cross.
- At meter P30 read the current consumption of the amplifier modules;
  at P_{RF} = 50 kW and m = 0: approx. 100 A per amplifier cabinet.

Check the phase display at meter P40:

- If the output filter is correctly tuned, the display should show + 7 scale divisions (the value is dependent on antenna or dummy load matching).

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14.3 Tuning the Transmitter

The transmitter is tuned in two steps:

1.) Coarse tuning: the transmitter is tuned with the aid of the current (P30: nominal value 100 A, switch S2 in position 1 and 2 for both amplifier cabinets)-, power (P10: nominal value 50 kW)- and tuning (P40) meters.

2.) Fine tuning: the transmitter is tuned with the modulation signal such that the AF frequency response is as flat as possible.

14.3.1 Coarse Tuning

The transmitter is first tuned without modulation at P2 (50 kW), i.e., the AF patch plug is not inserted in the front panel.
The transmitter is connected to an antenna.
The capacitors C53401 and C53801 are set to the factory value by rotating the capacitor adjustment knob:

(Key P2 - power stage 2 - is still switched on, green LED ”P2” is on, key ”PDM ON" is still switched on, green LED ”PDM ON” is on.

Should the transmitter shut down via a tuning trip when the PDM pulses are released, rotate the knobs of capacitors C53401/C53801 two revolutions to the left and switch on the transmitter again. If the transmitter again shuts down via a tuning trip, rotate the knobs of capacitors C53401/C53801 two further revolutions to the left.

The needle of the tuning (phase) meter should show a value of +7 scale divisions when the transmitter is properly tuned. This is carried out with the adjustment knobs of capacitors C53401/C53801.

Aside from the phase tuning, capacitors C53401/C53801 are used to adjust the current I to approx. 100 A per amplifier cabinet at a P_{RF} of about 50 kW / m = 0.

14.3.2 Fine Tuning

Fine tuning is carried out by modulating the transmitter with 1 kHz and 4 kHz. This requires connecting a audio frequency generator to the transmitter (AF input socket in the control panel). The low-pass filter in the transmitter is switched off. The transmitter is modulated to 50% with 1 kHz and subsequently at a constant AF input level, modulated with 4 kHz. At correct tuning, a modulation factor of m = 47% is

measured (modulation factor measurements with a test instrument connected to the RF test point or with meter P50, slide-switch S4 to the right).
Should the deviation of the modulation factor lie outside the range of the above value then the following transmitter fine tuning is to be carried out.

If the modulation factor at 4 kHz is:

m < 47%: turn knobs on capacitors C53401/C53801 to the right until $m_{(4kHz)}$ is approx. 47% at the same time hold the phase tuning to +7 scale divisions using these capacitors.

m > 47%: turn knob on capacitors C53401/C53801 to the left until $m_{(4kHz)}$ is approx. 47% at the same time hold the phase tuning to +7 scale divisions using these capacitors.

The desired value for phase tuning is about +7 scale divisions at P_{RF} = 50 kW.

After switching over to full power (100 kW) using key P1, the following values should be read at the respective meters:
U = 270 V / I = 100 A per amplifier cabinet and φ = 10 scale divisions.

14.4 Setting the Output Power in AM and DAM

- Press key P1 (power stage 1). The power has been factory set to P_{RF} = 100 kW.
- Green LED ”P1” lights up.
- The cross-point meter P10 reads 100 kW output power.
- Meter P30 displays the current consumption of the amplifier modules (at P_{RF} = 25 kW / m = 0: approx. 200 A per amplifier cabinet).
- Connect an audio frequency generator to the transmitter (AF input connector in the control panel)
- Modulate the transmitter with 1 kHz, m = 1.
- Meter P30 displays the current consumption of the amplifier modules (at P_{RF} = 100 kW / m = 1: approx. 300 A per amplifier cabinet).
- When VSWR and phase tuning are within tolerance, operation with AM program modulation can begin.
- Continue to modulate the transmitter with a 1 kHz Sine wave at 100 % modulation.
- During AM modulation press the ”DAM” key: green LED in the ”DAM” key lights up, green LED in the ”AM” key turns off, all other displays remain unchanged.
- Disconnect the modulation feed from the AF input connector.
- Meter P50 drops to 0 % modulation.
- RF output power display in cross-point meter P10 drops to about 36 kW
  Factory setting for DAM: ~60 % residual carrier voltage, ~36 % carrier power. It is possible to set other values by adjusting potentiometer R60 on the AF stage (rear side of the control panel).
- Insert the AF patch plug in the control panel and modulate the transmitter with a program signal.
- RF output power display in cross-point meter P10 varies as a function of the modulation between residual carrier power and nominal carrier power.
- Select the desired low-pass filter: LP 1: 4.5 kHz filter (-3dB), LP 2: 6.75 kHz filter (-3dB)
- The transmitter is ready for AM or DAM operation:
- P 1: The carrier power can be set between P_{RF} = 100 kW and P_{RF} = 50 kW by potentiometer R8 in control board.
- P 2: The carrier power can be set between P_{RF} = 50 kW and P_{RF} = 25 kW by potentiometer R6 in control board.

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14.5 Setting Instructions for the Output Monitor

Note: The jumper settings below are carried out at the connectors of the output monitor board in the control cabinet.

14.5.1 Power Display (Cross-point Meter)

Switch on the transmitter (P/1, m = 0) and measure the output power. **Switch off the transmitter each time before resetting jumpers**.

X40: jumper on pins 1/3, 2/4, 5/7 and 6/8.

Adjust R161 so that the cross-point meter displays the correct power.

X40: jumper on pins 1/2, 3/4, 5/6 and 7/8.

Adjust R160 so that the cross-point meter displays the correct power.

X40: jumper again on pins 1/3, 2/4, 5/7 and 6/8.

Adjust R161 so that the cross-point meter displays the correct power.

14.5.2 S-Shutdown Threshold and S-Power Reduction

At zero power, turn potentiometer R150 as far to the left so that no fault indications can occur. This setting has the effect that at low transmitter power, the power coupled in from the antenna does not cause a fault indication and if necessary the setting must be readjusted when the transmitter is operating on the antenna.

X5, X6, X16 and X33: Jumper across pins 2/3.

Turn R27, R28 and R139 fully clockwise.

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14.5.3 S-much-too-high Shutdown / s >>, (s = 2.0)

Switch transmitter to OFF.

X40: jumper across pins 1/3 and 5/7. Connect a power supply unit (0-5 Volt) to pin 4 (+pole) and pin 8 (-pole).

Switch transmitter to ON (P/1, m = 0).

Adjust the voltage at pin 4, 8 so that the cross-point meter shows s = 2.0.

Turn R139 to the left until the shutdown threshold is reached.

Control:

- Set voltage at pin 4, 8 to 0 V, clear fault indication at the transmitter.
- Increase voltage at pin 4, 8. Shutdown must occur when the cross-point meter shows s = 2.0.
- If necessary, correct the shutdown threshold with R139.

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14.5.4 S-too-high Shutdown / s >, (s = 1.55)

Switch transmitter to OFF.

X40: jumper across pins 1/3 and 5/7. Connect power supply unit (0-5 Volt) to pin 4 (+pole) and pin 8 (-pole).

Switch transmitter to ON (P/1, m = 0).

Adjust the voltage at pin 4, 8 so that the cross-point meter shows s = 1.55.

Turn R27 to the left until the shutdown threshold is reached.

Control:

- Set voltage at pin 4, 8 to 0 V, clear fault indication at the transmitter.
- Increase voltage at pin 4, 8. Shutdown must occur when the cross-point meter shows s = 1.55.
- If necessary, correct the shutdown threshold with R27.

14.5.5 S-Power Reduction / P(s), (s = 1.35)

Switch transmitter to OFF.

X40: jumper across pins 1/3 and 5/7. Connect power supply unit (0-5 Volt) to pin 4 (+pole) and pin 8 (-pole).

Switch transmitter to ON (P/1, m = 0).

Adjust the voltage at pin 4, 8 so that the cross-point meter shows s = 1.35.

Turn R28 to the left until the power reduction threshold is reached.

Regulate the voltage at pin 4, 8 so that during power reduction the shutdown threshold s = 1.55 is not exceeded.

Set the reduced power level with R131 (e.g. P/4). Fully clockwise = no reduction.

Control:

- Set voltage at pin 4, 8 to 0 V, clear fault indication at the transmitter.
- Increase voltage at pin 4, 8. Power reduction must start when the cross-point meter shows s = 1.35. If necessary, correct threshold with R28

After settings are completed, re-plug jumpers on X40 again across pins 1/3, 2/4, 5/7 and 6/8.

14.5.6 Power-too-low Shutdown

Switch transmitter to OFF.

Disconnect connector X7 on the output monitor.

X9: jumper across pin 1/2.

X40: jumper across pins 2/4 and 6/8. Connect power supply unit (0-5 Volt) to pin 1 (+pole) and pin 5 (-pole).

Turn R30 fully anti-clockwise.

Adjust the voltage at pin 1, 5 so that the cross-point meter shows the power at which shutdown should occur (half the output power).

Switch transmitter to ON (P/1, m = 0); (cross-point meter still shows half power).

Turn R30 slowly clockwise until the threshold is reached.

Control:

- Adjust the voltage at pin 1, 5 so that the cross-point meter shows full power. Clear the fault indication at the transmitter.
- Regulate down the voltage at pin 1, 5. Shutdown must take place when the cross-point meter shows half power. If, necessary, correct the threshold with R30.

Reconnect X7 and re-plug jumpers again at X40 (pin 1/3, 2/4, 5/7, 6/8).

14.5.7 Indication RF Present

Switch transmitter to OFF.

Disconnect connector X7 on the output monitor.

X1 and X8: jumper across pins 1/2.

X40: jumper across pins 2/4 and 6/8. Connect power supply unit (0-5 Volt) to pin 1 (+pole) and pin 5 (-pole).

Turn R29 fully clockwise.

Adjust the voltage at pin 1, 5 so that the cross-point meter shows the power at which the indication "RF Present" should be issued (about 7 kW).

Turn R29 slowly anti-clockwise until the indication "RF Present" is signaled.

Control:

- Set voltage at pin 1, 5 to 0 V.
- Increase the voltage at pin 1, 5. The indication must be displayed when the cross-point meter shows about 7 kW power. If necessary, correct threshold with R29.

Reconnect X7 and re-plug jumpers again at X40 (pin 1/3, 2/4, 5/7, 6/8).

14.5.8 Setting of $U_{discriminator}$

The voltage $U_{discriminator}$ is formed by the difference of the voltages delivered by the discriminator. It acts on the indications "tuning real" and "tuning capacitive" of the output monitor and serves to drive the phase display for the purpose of tuning the harmonic filter. This voltage cannot be set at the output monitor but only at the discriminator.

14.5.9 Tuning-Real-Warning (settings at the output monitor)

Turn potentiometer R41 on the control board so that it is approx. in the middle position.
Disconnect connector X15 from the output monitor.
X14: jumper across pins 2/3.
Connect power supply unit (0-5 Volt) to MP16 (-pole) and MP17 (+pole).
Turn R107 fully clockwise.
Switch transmitter on but with PDM inhibit (OFF).
Set the voltage at MP16/17 so that the phase meter shows -1 scale division.
Turn R107 slowly anti-clockwise until the warning indication LED (H21) "Tuning real" turns on.
Control:

- Set voltage at MP16/17 to 0 V. Clear the fault indication at the transmitter.
- Increase the voltage at MP16/17. LED H21 must turn on when the phase meter shows -1 scale divisions and must turn off at a reading of 0 scale divisions.
- If necessary correct the warning threshold with R107.

Reconnect X15.

14.5.10 Tuning-Capacitive-Shutdown (settings at the output monitor)

Turn potentiometer R41 on the control board so that it is approx. in the middle position.
Disconnect connector X15 from the output monitor.
X13: jumper across pin 2/3.
Connect power supply unit (0-5 Volt) to MP16 (-pole) and MP17 (+pole).
Turn R108 fully clockwise.
Switch transmitter on but with PDM inhibit (OFF).
Set the voltage at MP16/17 so that the phase meter shows -5 scale divisions.
Turn R108 slowly anti-clockwise until the indication "Tuning capacitive" LED (H39) turns on.

Control:

- Set voltage at MP16/17 to 0 V. Clear the fault indication at the transmitter.
- Increase the voltage at MP16/17. LED H39 must turn on when the phase meter shows -5 scale divisions and must turn off at a reading of 0 scale divisions.
- If necessary correct the warning threshold with R108.

Reconnect X15.

15. MAINTENANCE

15.1 General

The transmitter is so designed that when proper procedures for normal maintenance and control work are followed there is no risk of personnel coming into contact with parts under high voltage. **Safety Devices** present such as:

- **Key interlock**
- **Disconnect switches**
- **Emergency Cut-off Switch**

must be used in accordance with good electrical engineering practice. For detailed information, refer to the yellow safety pages at the beginning of this technical documentation.

15.1.1 Emergency Cut-off Switch

The **EMERGENCY CUT-OFF SWITCH** can be actuated in emergency situations to isolate the transmitter from power.

W a r n i n g !

Protection- or safety equipment must never be dismantled or made inactive.

The functioning of the emergency cut-off switch should be checked in half-yearly intervals.

15.2 Fan Tray Unit

The fan-tray unit should be checked at regular intervals to ensure that the fans run evenly and for abnormal bearing noise. The fans are, in principal, maintenance free. The normal operating life of the fans is approximately 10 years. Depending on the environmental conditions in which the transmitter is operating, the fan blades are to be inspected in half-yearly intervals for dust contamination and cleaned if necessary.

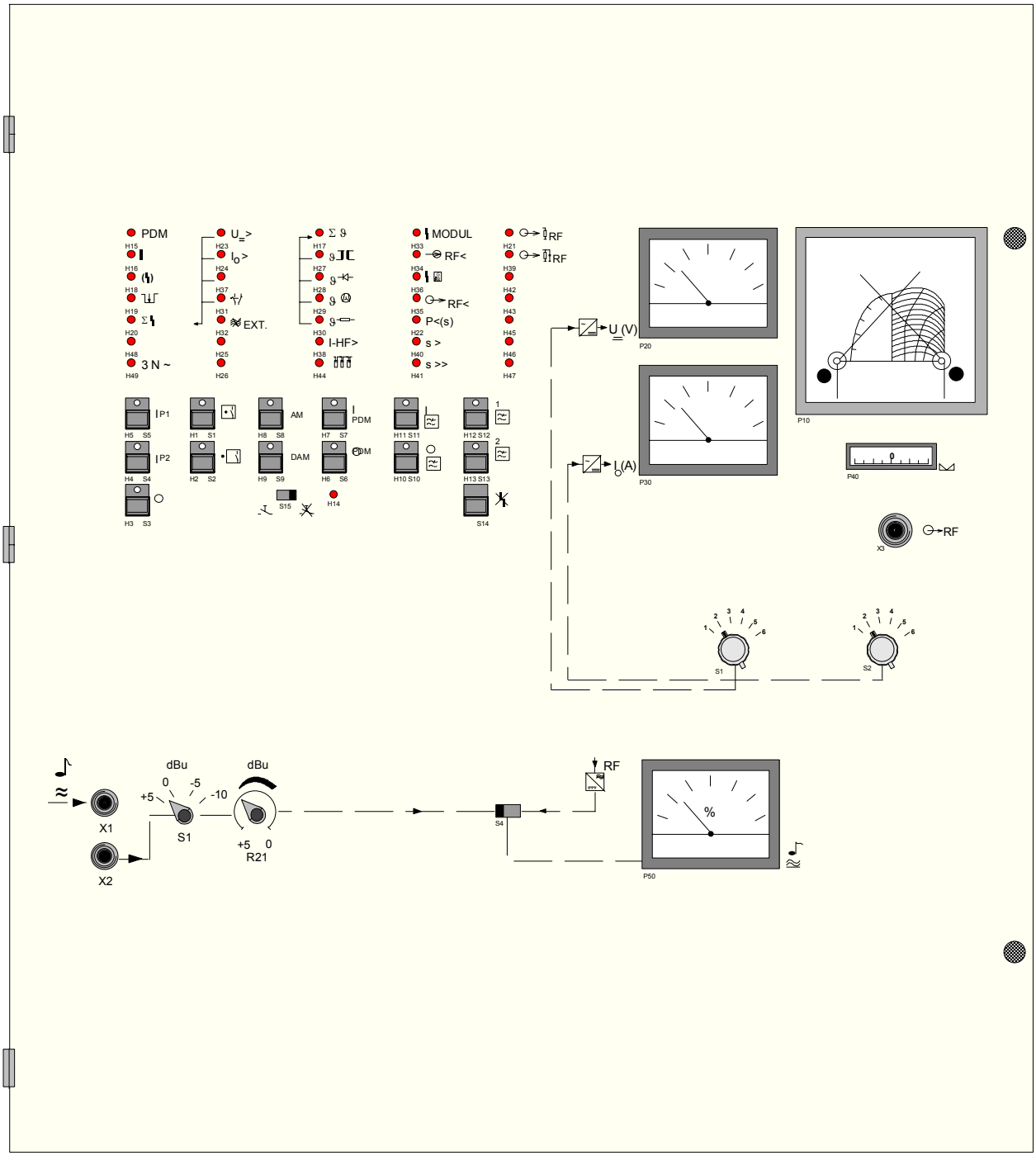
15.3 Electrical Connections

As part of routine maintenance work on the transmitter we recommend that all grounding connections as well as parts conducting high currents such as busbars are cables, for example, at the loadbreak switch (incoming and outgoing power cables) are checked for proper connection i.e., screws firmly fixed and re-tighten if necessary.

Special attention should be paid to the clamping screws at the loadbreak switch that they are firmly tightened.

In addition to the routine work, a check of electrical connections should also be made after any repair work on the power distribution system.

Control Panel



Front View

The transmitter is operated and monitored from the control panel. Transmitter indications (faults and normal operating conditions) are signaled by LEDs. Pushbutton keys are used to set the desired operating state. Meters display transmitter output power, mismatch, phase and modulation, as well as the operating voltage of the amplifier modules and their current consumption.

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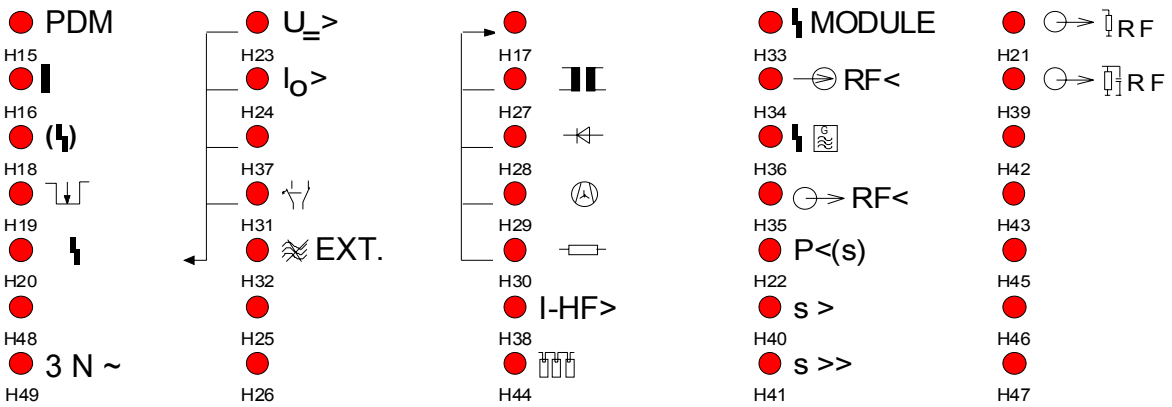
Light Emitting Diodes (LEDs)



LED	Meaning	LED	Meaning	LED	Meaning	LED	Meaning
H 15	PDM Enable	H 23	Supply voltage for the amplifier cabinet too high	H 17	Summary fault (for faults signaled by LEDs H 27, H 28, H 29 and H 30)	H 33	Fault in the amplifier modules
H 16	Transmitter ON (main contactor)	H 24	Current consumpt. of the amplifier cabinet too high	H 27	Overtemperature, transformer in amplifier cabinet	H 34	RF drive signal too low
H 18	Warning	H 37	not used	H 28	Overtemperature, diodes on the rectifier board	H 36	Oscillator fault
H 19	Continuous blocking	H 31	Automatic cutout tripped (auxiliary contact)	H 29	Overtemperature in amplifier cabinet (air cooling)	H 35	RF output power too low
H 20	Summary fault (for faults signaled by LEDs H 23, H 24, and H 31)	H 32	External carrier loop (open)	H 30	Overtemperature of the charging- and discharging resistors	H 22	Power reduction due to high mismatch (s >)
H 48	not used	H 25	not used	H 38	Overcurrent in the combiner assembly	H 40	Shutdown due to high mismatch (s >)
H 49	Mains power OK (indication from phase monitor)	H 26	not used	H 44	PC board loop (open)	H 41	Fast shutdown due to very high mismatch (s >>)
						H 21	Load real
						H 39	Load capacitive

The LEDs H 25, H 26, H 37, H 42, H 43, H 45, H 46, H 47, H 48 held in reserve (not used).

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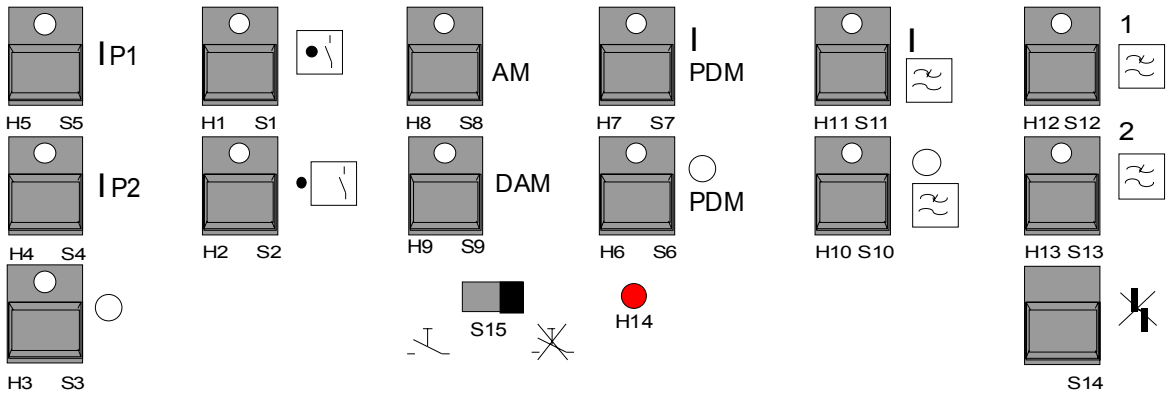
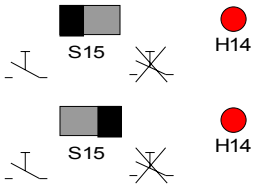
Pushbutton Keys, Slide Switches and Meters



Key LED	Assignment	Key LED	Assign-ment	Key LED	Assign-ment	Key LED	Assign-ment	Key LED	Assignment	Key LED	Assign-ment
S 5 H 5	Tx ON (full power P1)	S 1 H 1	Local control	S 8 H 8	AM	S 7 H 7	PDM ON	S 11 H 11	Low-pass filter ON	S 12 H 12	Select: low-pass filter 1
S 4 H 4	Tx ON (reduced power P2)	S 2 H 2	Remote control	S 9 H 9	DAM	S 6 H 6	PDM OFF	S 10 H 10	Low-pass filter OFF	S 13 H 13	Select: low-pass filter 2
S 3 H 3	Tx OFF									S 14	Clear fault indication

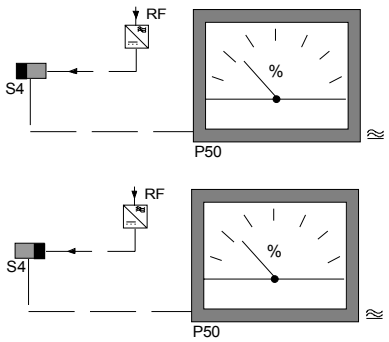
Slide switch S 15



Left position: Keys enabled

Right position: Keys inhibited. This state is signaled by LED H14 .

Slide switch S 4 switches over the modulation display at meter P50.



Left position: Display of modulation at the transmitter input

Right position: Display of modulation at the transmitter output

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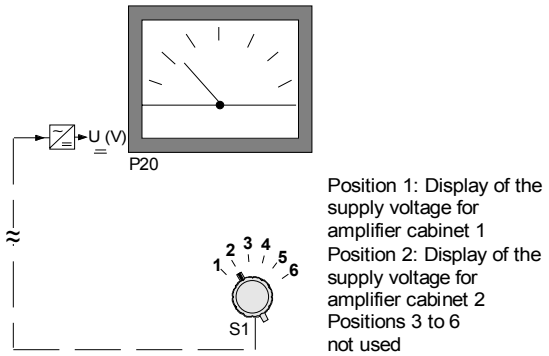
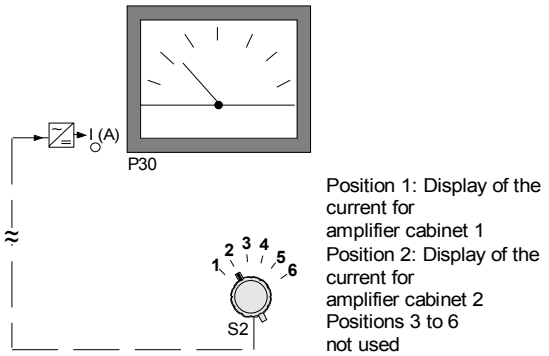
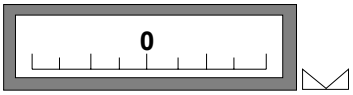
Switches S1 and S2 are used to select the amplifier cabinet for the display of supply voltage and current at meters P20 and P30 respectively.



Position 1: Display of the supply voltage for amplifier cabinet 1
Position 2: Display of the supply voltage for amplifier cabinet 2
Positions 3 to 6 not used



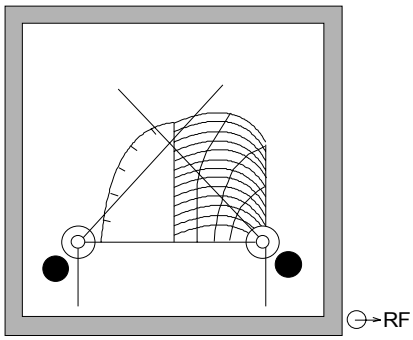
Position 1: Display of the current for amplifier cabinet 1
Position 2: Display of the current for amplifier cabinet 2
Positions 3 to 6 not used



P40

Phase Meter P40

The value is dependent on antenna/dummy load matching.



P10

Cross-point Meter.

The output power and mismatch are read off at the position where both pointers cross.

Horizontal lines = output power

Vertical lines = mismatch

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Fault Table: Power Supply

LED	Fault Indication	!	Hazard	Effect	Cause	Comment
H 23	Supply voltage too high U>	S	- Danger to amplifier modules due to overvoltage	- Shutdown	- Overvoltage in mains supply - Transformer incorrectly tapped on the primary side	- Check transformer and if necessary retap
H 24	Current consumption too high I>	S	- Danger to rectifier due to overcurrent	- Shutdown	- Short circuit in amplifier module supply - Faulty transmitter- antenna matching	- Check power busbars - Check matching
H 17	Summary fault Overtemperature	S	- Overloading components	- Shutdown	- See overtemperature indications below	- Evaluate temperature faults
H 27	Overtemperature Transformer	S	- Overloading the transformer	- Shutdown	- Rectifier defect - Short circuit in transformer and/or the cabling	- Check transformer and rectifier
H 28	Overtemperature Rectifier	S	- Overloading the rectifier	- Shutdown	- Rectifier defect - Cooling defect	- Check rectifier assembly
H 30	Overtemperature Resistor	S	- Overloading the charging- / discharging resistors	- Shutdown	- Overheating the resistors due to repeated TX on/off switching	- Visual inspection of resistors
H 31	Automatic cutout, trip	S		- Shutdown	- Automatic cutouts tripped and/or contactor defect or not engaged	- Check low voltage distribution

Fault Table: RF Processing, RF Amplifier, RF Output Monitoring

LED	Fault Indication	!	Hazard	Effect	Cause	Comment
H 34	RF drive power too low	D		- Shutdown	- Drive level too low or missing	- Check RF driver
H 44	PC Board Interlock			- PDM pulses are blocked - 'PDM ON' lamp turns off	- One or more RF modules missing - Fault in signaling connections - PC boards interchanged	- Check slide-in modules and connections
H 33	Modules	W		- Lower RF output level	- At least one module is defective	- Evaluate LED lamps in the modules
H 35	RF output power too low	D	- Possible overloading of the amplifier stage	- Shutdown	- Fault in power supply - Tuning fault - Module(s) failure - RF driver defect - PDM drive for RF driver and/or amplifier stage missing	- Check the listed points
H 22	Power reduction due to high mismatch (s >)	W		- Tx regulates the output power down to the set threshold	- Mismatch due to antenna- and/or feed line fault	- Check antenna and connectors - Tx operates at reduced power
H 40	Shutdown due to high mismatch (s >)	D	- Overloading of amplifier modules	- Shutdown	- Mismatch due to antenna- and/or feed line fault	- Check antenna and connectors
H 41	Fast shutdown due to very high mismatch (s>>)	D	- Overloading of amplifier modules - Flashover	- Shutdown	- Mismatch due to antenna-, feed line fault - Lightening strike	- Check antenna and connectors

Fault Table: AF Indications, Tx System Protection

LED	Fault Indication	!	Hazard	Effect	Cause	Comment
H 38	Overcurrent in the combiner assembly I - HF >	D	- Danger due to flashovers	- Shutdown	- Mismatch, flashover in output filter	- Check amplifier stage for burn marks
H 32	External carrier loop	P		- Pulses blocked as long as carrier blocking loop is open	- Operation inhibited by TX system protection	- Check carrier blocking loop
H49	Interruption to mains supply	U	- Station power supply fault	- Shutdown, automatic reconnection when mains OK.	- Phase problem	- Check station power supply (circuit breakers)

Legend: W = Warning; S = Summary Fault; D = Continuous Blocking; P = PDM blocking; U = Interruption

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